

Validation and Test Generation for Inductance Induced Noise on VLSI Interconnects

Arani Sinha, Sandeep K. Gupta and Melvin A. Breuer

Dept. of EE-Systems, University of Southern California, Los Angeles, CA 90089.

{sinha, sandeep, mb}@poisson.usc.edu

1. Introduction

Advancements in integrated circuit technology have led to an increase in switching speeds of digital circuits. This increase is the primary reason why inductance induced noise (e.g., oscillation, delay, crosstalk) is beginning to cause chips to fail [3]. Thus, we now see a great interest in the inductance associated with on-chip signal lines [2]. Validation and test issues related to capacitive crosstalk noise in integrated circuits have been addressed [1]. However, test issues pertaining to inductance induced noise have not been dealt with. In this paper, we address issues pertaining to test and validation of inductance induced noise associated with interconnects. The noise generated at a noise-site may propagate to a primary output or a latch input and create logic-value errors. *This motivates the validation problem.* An aggressive design may not exhibit noise problems for nominal set of process parameters but may exhibit a large amount of noise in a fabricated circuit due to process variations and spot defects. *This motivates the test generation problem.*

For our studies, we have used a 0.18 μm copper process from UMC, a fabrication facility in Taiwan. The capacitance and resistance values of the interconnects at a DC voltage are used. The self inductance of an interconnect (and the mutual inductance between interconnects) is extracted when the interconnect (or a set of interconnects) is surrounded by a ground and power mesh. It is assumed that the current returns through the entire mesh. The tool *FASTHENRY* is used for extracting inductance [6]. Circuit parameters and edge-rates of signals for each experiment is not discussed for reasons of space, but mentioned only when it would give an idea of the nature of circuits used for these studies.

2. Noise characteristics

2.1. Inductance induced noise

Crosstalk pulse: Two adjacent interconnects are used to study crosstalk induced pulses. The aggressor is driven by a strong driver, and the victim is driven by a weak driver. Medium sized receivers are used. Each line is 3 μm wide and separated by 0.24 μm . The line length is 3000 μm . The self and mutual inductances are 0.7 pH/ μm and 0.4 pH/ μm , respectively. The self and mutual capacitances are 150 aF/ μm and 80 aF/ μm , respectively. The line resistance is 4m Ω / μm . The input to the aggressor is switched from low to high, and the input to the victim is held constant at 0 V. The following two cases are considered: (i) all inductances of the interconnects are ignored, and (ii) all inductances are considered. A crosstalk pulse is induced on the victim line due to a transition on the aggressor line. The crosstalk pulse in case (ii) is slightly oscillatory. For certain other combinations of circuit parameters, the crosstalk pulse can be very oscillatory. In this case, it is found that the peak magnitude of the pulse is 0.8V, which is more than eight times the peak magnitude of the pulse in the first case. This experiment demonstrates that crosstalk induced by a combination of mutual inductance and mutual capacitance can be higher than that due to capacitive coupling alone.

Crosstalk speedup and slowdown: The same circuit is used to study crosstalk speedup. Two values of separation between the interconnects are used: (i) 1 μm , and (ii) 3.5 μm . When the separation is 1 μm , the mutual capacitance and the mutual inductance between the two interconnects are 25aF/ μm and 0.38pH/ μm . The difference in delay, i.e., the speedup in a transition at the output of the victim receiver when the aggressor is not switched versus when it is switched in the same direction is 125 ps. When the separation is 3.5 μm , the mutual capacitance and the mutual inductance values are 1 aF/ μm and 0.32pH/ μm . Now the mutual inductance has a moderate value but the mutual capacitance is very low. For this case, the delay at the victim output is higher by about 15% (10 ps) when both inputs switch in the same direction. This is an instance of crosstalk slowdown. This phenomenon has been observed in [4]. The physical explanation for speedup and slowdown is that a purely inductive (mutual capacitance ignored) crosstalk effect and a purely capacitive (mutual inductance ignored) crosstalk effect are primarily in opposite phases to each other, and based on the relative values of mutual inductances and capacitances, one or the other dominates. Similar effects exist when the input signals have opposite transitions. A design rule frequently employed to reduce capacitive crosstalk delay is to increase the separation between interconnects. These experiments demonstrate that for interconnects whose inductance cannot be ignored, the delay problem will be encountered even if the spacing between adjacent interconnects is increased.

Oscillatory noise: For this experiment, only a single interconnect is considered. Again, a strong driver and a medium sized receiver is used. Since for realistic values of self-inductance, the oscillatory noise is low, we increased the magnitude of the inductance by a factor of three. We believe that such noise will be prominent as we move into deeper sub-micron processes where transistors are much more sensitive to noise. Since we do not have data for such processes, we have tried to study the effect by increasing the magnitude of the inductance. The output of the victim driver and receiver have an oscillatory transition when the input has a ramp transition. The magnitude of the first undershoot at the receiver output exceeds the threshold voltage by about 50%.

Combination of oscillatory noise and crosstalk: For certain values of skew between the signals on the aggressor and the victim, the oscillatory noise can combine with crosstalk noise in a manner that increases the severity of the total noise. A circuit similar to the one used to study crosstalk pulse magnitude is used, with the alteration that the magnitude of all inductances are increased by a factor of three. The following cases are considered: (i) the aggressor is not switched, (ii) the aggressor is switched in the opposite direction to the victim and with a skew of 50ps, (iii) same as (ii) but the skew between signals is 100 ps, and (iv) same as (ii) but the skew between the signals is 150 ps. For all cases, the output of the victim receiver has some oscillation. For case (i), the maximum value of the undershoot is negligible. For the remaining cases, there is one undershoot with a high

value, which is a function of skew. The largest value of the undershoot occurs for case (iii), and is 1.08 V.

2.2. Interconnect length

The impact of interconnect length on (i) crosstalk pulse, and (ii) oscillatory noise was studied. It has been argued that noise is an issue in global interconnects and not in local and medium-length interconnects. Because we are interested in testing combinational blocks, the interconnects that occur in such blocks are not very long. One question is whether noise in such blocks is a validation and test issue. In the next series of experiments, the line length was increased from 1000 μm to 10,000 μm . We observe that the magnitude of the pulse (for crosstalk noise) and the magnitude of the undershoot (for oscillatory noise) first increases and then decreases. For case (i) the magnitude of the crosstalk pulse is about twice the threshold voltage when the line length is 2000 μm , and the maximum occurs for a line length between 3000 μm and 4000 μm . This maximum value is about 2.5 times the threshold voltage. For case (ii), the maximum occurs for 2000 μm , and is about 1.6 times the threshold voltage. It is reasonable to assume that the longest interconnects in combinational logic blocks are about 2000 μm long. Thus, such noise can occur on interconnects in combinational blocks, whose validation and test is of concern.

2.3. Signal edge-rate and skew

The impact of edge-rate on (i) crosstalk pulse, and (ii) oscillatory noise are considered. For each of these two cases, the maximum magnitude of the noise increases with decreasing edge-rate. This noise will probably increase in the future, since switching rates are expected to become faster. However, it is not true that such noise will increase monotonically with switching rates for all circuit configurations [5].

The combined impact of edge-rate and skew on crosstalk delay was also studied. The edge-rate of the input signal to the victim driver is 100ps. The edge-rate of the aggressor driver and the skew between the two signals were altered. The skew was varied from -200 ps to 300ps. The edge-rate was changed from 0ps to 200ps. The variation in delay is about 5% (32 ps) about the mean delay. For certain other combinations of circuit parameters, larger variations in delay have been noticed. Also in this case, the delay varies non-monotonically with the values of edge-rate and skew.

For each of these types of noise, the combination of edge-rate and skew that results in maximum noise or delay can be different for different aggressor/victim pairs. The optimal test vectors used to excite and detect such noise effects should try to excite the best value of the combination of edge-rate and skew.

3. Spot defect and process variation

Spot defects such as those that reduce the strength of the victim driver can increase the magnitude of the crosstalk pulse at the victim output. For a specific circuit in which the strength of the victim driver was reduced to half its original value, the magnitude of the crosstalk pulse increased by a factor of two.

The impact of process variation was studied next. It is assumed that two different and uncorrelated sources of process variation are present: (i) the sheet resistance of the interconnect, and (ii) the gain factors of the transistors. Three different realistic values of sheet resistances are used. It is assumed that all other circuit parameters remain the same. Five different process corners for transistors are used: (i) typical p -transistor and typical n -transistor corner (or typical-

typical corner), (ii) fast-fast corner, (iii) slow-slow corner, (iv) fast-slow corner, and (v) slow-fast corner. These lead to fifteen different combinations. The maximum magnitude of the crosstalk pulse occurs for the minimum value of sheet resistance and the slow-fast corner. This value is more than 50% higher than the nominal value. This experiment shows that process variation has a huge impact on crosstalk.

4. Pattern dependence

In this section, we study how the magnitude of noise is affected by input stimulus applied to a circuit. The aggressor input is switched, the victim input is held constant at 0 V. The magnitude of crosstalk pulse at the victim output is measured under two conditions: the input to a second aggressor line adjacent to the victim is (i) held constant at 0 V, and (ii) held constant at 1.5V.

For case (i), the magnitude of the pulse is larger than for case (ii) by about 30%. This experiment demonstrates that the value on a non-switching adjacent interconnect can affect the magnitude of noise. This is caused by a difference in the value of the transfer function at the victim output.

5. Conclusions

It is seen that inductance in VLSI interconnects can lead to various problems. Severities of many of these problems are expected to increase in the future. These problems are significant even for medium-length interconnects and therefore test and validation issues for medium-length interconnects in combinational blocks should be addressed. Even though it is not likely that inductances can be affected by process variations (because dimensions of large return loops may not be significantly affected), inductance induced noise is significantly affected by process variations and spot defects because of changes in other circuit parameters.

From a test generation perspective, the vector should excite the noise-site with a combination of edge-rate and signal skew such that the worst possible noise or delay is created, subject to propagation conditions. Also, interconnects with static signals adjacent to noise site should be excited such that the noise effect is maximized. We plan to include these two issues in a mixed-signal test generator for noise being developed at the University of Southern California.

Acknowledgement: The authors would like to thank UMC for providing process files for their 0.18 μm copper process. Thanks are also due to the authors of the tool *FAS-THENRY* for making the software available publicly.

6. References

- [1] Chen, W. Y., Gupta, S. K., Breuer, M. A.: Test generation in VLSI circuits for crosstalk noise, *Proc. of Int'l. Test Conf.*, pp. 641-650, 1998.
- [2] Deutsch, A. et al.: When are transmission line effects important for on-chip interconnections?, *IEEE Trans. on Microwave Theory and Techniques*, Vol. 45, No. 10, pp. 1836-1846, Oct., 1997.
- [3] Naffziger, S.: Design methodologies for interconnect in GHz+ ICs, *Tutorial in Intl. Solid-State Circuits Conference*, 1999.
- [4] Restle, P., Ruehli, A. and Walker, S. G.: Dealing with inductance in high speed chip design, *Proc. of Design Automation Conf.*, pp 904-909, 1999.
- [5] Kopsay, G. V.: Private communications.
- [6] Kamon, M., Tsuk, T. J., White, J. K.: FASTHENRY: A Multi-pole Accelerated 3-D Inductance Extraction Program, *IEEE Transactions on Microwave Theory and Techniques*, 42, No. 9, Sept. 1994.