

# Constraints for Using IDDQ Testing to Detect CMOS Bridging Faults\*

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## Abstract

Detecting CMOS bridging faults (BFs) using IDDQ testing, or the current supply monitoring method (CSM), has recently received much attention. One fundamental question that needs to be answered for this technique is "what circuits does it apply to". Previously we presented a set of constraints on circuits and their test environment that formed a sufficient condition for using CSM to detect all single and multiple irredundant BFs. In this paper we show that if any of these constraints are removed then circuits exist for which CSM cannot give correct results. Two special classes of circuits, domino logic and synchronous sequential circuits, are discussed in detail.

## 1 Introduction

Bridging faults (BFs) have been shown to be a major source of failure in VLSI circuits [1, 2]. Conventional methods for detecting BFs employ only *logic testing*, i.e., use *wired-OR* or *wired-AND* models for faults and monitor logic values (high or low) at the primary outputs (see, e.g., [3, 4]). The feasibility of logic monitoring has been examined by many researchers and it has been shown that logic testing is inadequate for detecting CMOS BFs that may result in indeterminate logic levels [5, 6, 7].

IDDQ testing, or the current supply monitoring method (CSM) [8, 9, 10], is an alternative approach for detecting BFs in CMOS circuits. This method takes advantage of an important property of CMOS circuits, namely during steady state the current supplied by the power source should be extremely small. When a BF exists between two nodes that are respectively connected to *VDD* and *GND* through conducting transistors, the supply current becomes quite large. By monitoring this current the fault can be detected.

Several circuit devices for measuring steady state current have been proposed [11, 12, 13, 14]. A new

testing methodology called *built-in current testing using built-in current sensors (BICS)* has been described in [13, 14]. By partitioning a circuit into modules and using a separate *BICS* for each module, this method not only facilitates on-line self-testing but also makes CSM applicable to large circuits. Thus CSM appears to be a promising method for detecting CMOS bridging faults.

The applicability of CSM, however, requires careful examination. Previously we have shown that many problems exist for CSM if it is not properly employed [15]. These problems include 1) a fault-free circuit may be identified as faulty; 2) even though in a fault-free circuit a test can connect two nodes to *VDD* and *GND*, respectively, this test does not necessarily detect a BF between these two nodes; and 3) a test for a single BF may be invalidated due to the existence of other BFs.

In [15] we also proposed a set of constraints on a circuit and its test environment. With these constraints it has been formally shown that all single irredundant BFs (BFs that cannot affect the logic function of a circuit) can be detected by CSM, and if a test vector detects a single BF, it also detects every multiple BF that contains this single BF. Thus these constraints form a sufficient condition for using CSM to detect CMOS bridging faults.

In this paper we further illustrate the importance of these constraints. It will be shown that if any of these constraints are removed, then circuits exist for which CSM will not give correct results. Thus our constraints can be considered or used as design and test rules for CMOS circuits to facilitate IDDQ testing.

To further explore the applicability of IDDQ testing, we have examined many circuits that do not satisfy some of the constraints. Due to space limitation, in this paper we shall only discuss two classes of these circuits, namely domino logic and synchronous sequential circuits. We shall analyze the problems that may occur when using IDDQ testing and provide suggestions and/or strategies for dealing with these problems. A detailed discussion on circuits not satisfying each of the proposed constraints can be found in [16].

The remainder of this paper is organized as follows. In Section 2 we review the previous work done in [15]. This includes the circuit model, the proposed

\*This work was supported by the Defense Advanced Research Projects Agency and monitored by the Office of Naval Research under Contract No. N00014-87-K-0861. The views and conclusions contained in this document are those of the authors and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the U. S. Government.

constraints and the derived theorems. In Section 3 we use examples to illustrate the importance of each proposed constraints. Various examples that satisfy all but one constraint are given. In Section 4 we analyze the problems in domino logic and sequential circuits, and provide suggestions and/or strategies for these problems. Concluding remarks are made in Section 5.

## 2 Preliminary work

### 2.1 Circuit model

A CMOS circuit consists of a number of  $n$ -type/ $p$ -type transistors and a number of nodes connecting these transistors. A commonly-used partitioning method for MOS circuits is adopted [17, 18]. This method partitions a circuit described at the switch level into a number of "channel-connected components" called *transistor groups (TGs)*. Figure 1 shows the partitioning of a circuit and some of its TGs. Each dotted polygon indicates a TG.

Each interconnection between TGs is unidirectional and can be considered as an *input* or *output* of the corresponding TGs. A transistor group  $TA$  can *control* another transistor group  $TB$  if one of the outputs of  $TA$  affects one of the inputs of  $TB$ . For example, in Figure 1  $TG_1$  can control  $TG_2$  and  $TG_3$ , and  $TG_2$  can control  $TG_3$ . If one TG can control another TG, then these two TGs are *related*, otherwise they are *unrelated*. If two TGs can control each other, then a *control loop* exists.

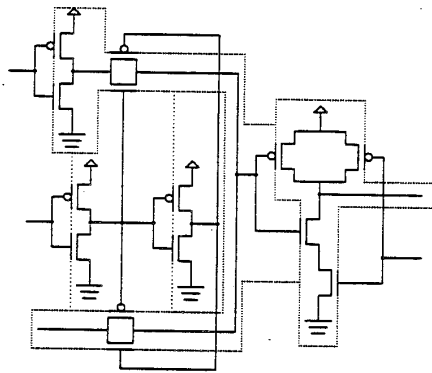


Figure 1: Partitioning of a CMOS circuit

### 2.2 Circuit constraints

The following constraints on a fault-free circuit and its test environment have been presented in [15].

- A1. The gate and drain (or source) node of a transistor cannot be in the same TG.
- A2. During steady state operation, there must be no conducting path from  $VDD$  to  $GND$ .

A3. During steady state operation, each output of a transistor group must be connected to  $VDD$  or  $GND$  through a path of conducting transistors.

A4. There are no control loops among TGs.

A5. The substrate (or well) of an  $n$ -type( $p$ -type) transistor is connected to  $GND(VDD)$ .

A6. During testing, each primary input is controlled by a strong power source whose current flow is also monitored.

The rationale of these constraints is briefly described below. A1 excludes the possibility of "self-control" inside a transistor group. A2 is a common attribute of CMOS circuits. A3 ensures that a circuit's normal operation does not rely on any "charge sharing" or "charge retention" effects. A4 assumes no feedback exists in the circuit. A5 ensures that a BF will not cause *anomalous reverse conduction* that may occur at the drain-substrate (or well) junction when the substrate is connected to the source [7, 19]. A6 makes sure that if a primary input is involved in a BF, it cannot stabilize at an erroneous logic values without consuming a large steady state current, and this abnormal current can be detected.

A1—A5 are constraints on circuits while A6 is a constraint on the test equipment. For brevity, rather than using the phrase "a circuit satisfies A1—A5 and the test environment A6 is set up for testing this circuit", we shall simply say that "a circuit satisfies A1—A6".

### 2.3 Fault classifications and derived theorems

A single bridging fault is allowed to occur between any two nodes in the circuit under consideration. These nodes include all PIs, POs, I/O of TGs and all internal nodes of TGs. When a BF occurs, it is assumed that the resistance between the two shorted nodes is 0. All single BFs in circuits that satisfying A1—A6 can be classified into three categories, namely (1) BFs inside a TG, (2) BFs between two unrelated TGs, and (3) BFs between two related TGs. A multiple BF is defined as a fault that consists of one or more single BFs. A BF is called redundant if it does not affect the logic function of a circuit.

The following basic approach is used to determine the applicability of CSM: *when an appropriate test vector is applied, if due to a fault there exists one or more paths from  $VDD$  to  $GND$  such that at any time at least one of these paths is conducting, then the fault is detected using CSM*. This approach ensures that CSM can detect a BF only if there exists conducting path(s) between  $VDD$  and  $GND$  all the time, not just temporarily. The following theorems have been proved in [15].

**Theorem 1** A single bridging fault in a circuit satisfying A1–A6 is either detectable by using CSM or is redundant.

**Theorem 2** If  $T_1$  is a test vector for a single BF  $f_1$ , then  $T_1$  is also a test vector for every multiple BF that contains  $f_1$ .

### 3 Importance of the constraints

Due to Theorems 1 and 2, the six constraints A1–A6 form a sufficient set of conditions for using CSM to detect all irredundant BFs. In this section we shall discuss the importance of each of these constraints via circuit examples.

**A1—drain (or source) and gate are not in the same TG** Consider the circuit shown in Figure 2 that contains two transistor groups  $TG_1$  and  $TG_2$ .  $TG_2$  violates A1 because the gate and drain nodes of the p-type and n-type transistors of the inverters driving  $y$  and  $z$  are in the same group. A2 is satisfied because no VDD-GND connection exists during steady state operation (the two pass transistors connected to  $O$  are controlled by complementary values). A4 is also satisfied because the loop containing  $y$  and  $z$  is an “internal loop” rather than a control loop. It is easy to verify that all other rules are/can be satisfied.

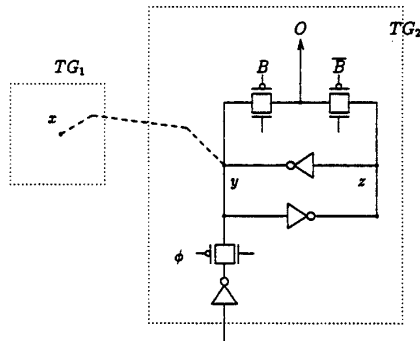


Figure 2: A circuit that violates only A1

Assume  $TG_1$  satisfies A1–A6 and there exists a BF between a node  $y$  in  $TG_2$  and a node  $x$  in  $TG_1$ . To detect this BF,  $x$  and  $y$  must be set to complementary values. If  $x$  and  $y$  become stable only when  $\phi = 1$ , then due to the “closed loop” containing  $y$ , during steady state  $y$  will reach the same logic value as  $x$  and no excess current will be observed [20]. Therefore CSM will fail to detect this fault.

**A2—no conducting path from VDD to GND** This constraint is essential since otherwise an excess current will exist in a fault-free circuit. Examples of this type of circuitry include pseudo-NMOS, pseudo-PMOS and BiCMOS circuits.

**A3—no floating output nodes** Refer to Figure 3. The MUX output  $O = O_1$  if  $Sel = 1$ , and  $O = O_2$  if

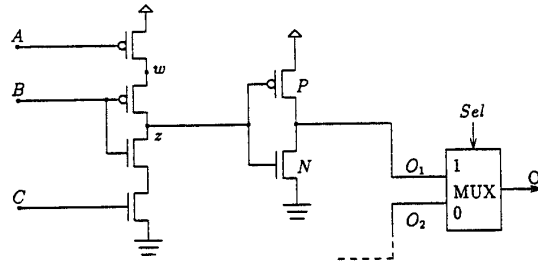


Figure 3: A good circuit that may be identified as faulty circuit

$Sel = 0$ . When  $ABC = 100$ , both  $w$  and  $z$  are isolated from VDD and GND. Since  $B = 0$ , charge sharing between  $z$  and  $w$  occurs and the resulting voltage value  $v$  depends on their previous states. It is possible that  $v$  may be greater than the threshold voltage of transistor  $N$  but not large enough to cut off the transistor  $P$  [21, 22]. Thus both  $P$  and  $N$  may conduct resulting in a large current through the inverter. Therefore the circuit may be identified as faulty when using CSM. However if the circuit is designed such that  $Sel = 0$  whenever  $ABC = 100$ , the circuit output is still correct if  $O_2$  is correct. This type of problem may occur when implementing a circuit whose I/O relation is not completely specified, e.g., when there exist *don't care* terms in the Karnaugh map.

**A4—no control loop** Consider the circuit shown in Figure 4(a) that contains a bridging fault ( $x, y$ ). Without ( $x, y$ ) we can set  $x$  and  $y$  to complementary values by setting nodes  $a$  and  $b$  to complementary values during  $\phi_1$ , and propagating these values to  $x$  and  $y$ , respectively, during  $\phi_1$ . The equivalent circuit of Fig-

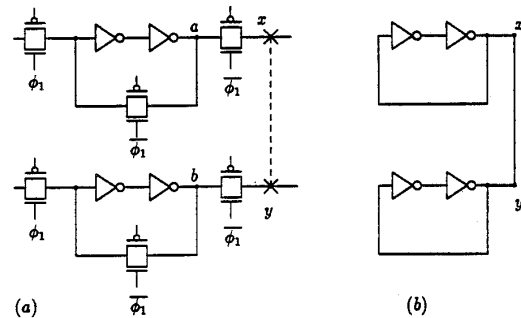


Figure 4: A BF that cannot be detected by just setting the two shorted nodes to complementary values

ure 4(a) during  $\overline{\phi_1}$  is shown in Figure 4(b). Because of ( $x, y$ ), the two loops containing  $x$  and  $y$  are connected together. Since there is no “external” control to these

two loops, once the transition from  $\phi_1$  to  $\overline{\phi_1}$  is made,  $x$  and  $y$  will rapidly reach the same stable state (either 0 or 1) and no large current can be observed during steady state [20]. Thus the fault  $(x, y)$  cannot be detected by CSM.  $\square$

**A5—substrate (or well) connected to VDD or GND** Consider the circuit shown in Figure 5(a) which contains a BF  $(x, y)$ . In a fault-free circuit if  $x = 0$  then  $y$  must be 0 and if  $x = 1$  then either  $y = 1$  or  $y$  is floating. Therefore no test can set  $x$  and  $y$  to complementary logic values and BF  $(x, y)$  is considered as redundant.

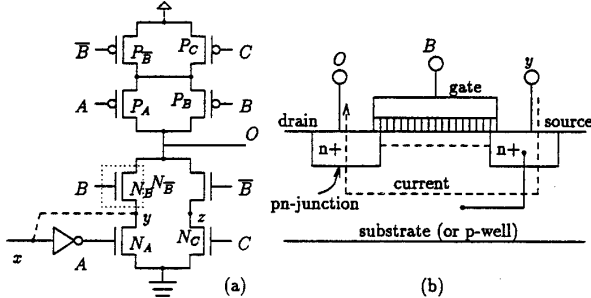


Figure 5: Anomalous reverse conduction

Now assume the substrate of transistor  $N_B$  is connected to its source node rather than  $GND$  as shown in Figure 5(b). When a vector  $xBC = 101$  is applied, node  $y$  and the substrate of  $N_B$  will be set to 1 due to  $(x, y)$ . Thus the pn-junction at the drain node ( $O$ ) will be forward biased because  $O$  is connected to  $GND$  through transistors  $N_{\overline{B}}$  and  $N_C$  and an anomalous reverse conducting path [7] forms from node  $x$ , through node  $y$ , the substrate of  $N_B$ , node  $O$ , node  $z$ , to  $GND$ . This results in an excess current. However classical test generation procedures will not generate a test for this fault since it is considered as redundant.

**A6—PI current monitored** If constraint A6 is not satisfied, then a bridging fault that involves a primary input may not be detected. Consider the circuit shown in Figure 6. To detect a BF  $(x, y)$  we must set  $x = 1$  and  $y = 0$  so that a large current from  $VDD$  through  $x, y$  to the driver of  $B$  can be generated in the faulty circuit. But since the current on line  $B$  is not monitored, the fault cannot be detected.

## 4 Case studies

We have shown that without any one of constraints A1-A6, CSM will have some problems. In this section we shall examine these problems in more detail. Due to space limitation, we will only examine two classes of circuits which represent typical circuits that do not satisfy A3 and A4, respectively.

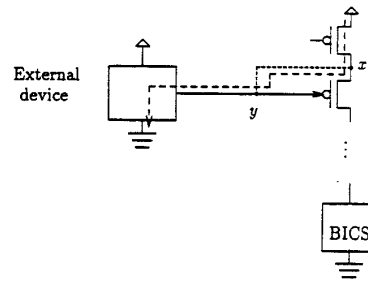


Figure 6: Importance of A6

### 4.1 Domino logic

Consider a domino logic gate that consists of a precharge stage and an inverter shown in Figure 7(a). For any BF  $(x, y)$ , if both  $x$  and  $y$  are inside the evaluation block, then during  $\phi = 0$  neither of these two nodes can be connected to  $GND$  and during  $\phi = 1$  neither of them can be connected to  $VDD$ . Thus it is impossible to connect  $x$  and  $y$  to complementary power sources at the same time. Hence  $(x, y)$  cannot be detected using CSM. Similarly, if  $x$  and  $y$  are in the evaluation blocks of two different precharge stages,  $(x, y)$  cannot be detected using CSM either. The only BFs that can be detected by CSM in domino logic are those involve  $VDD$ ,  $GND$  or the output nodes of the inverters.

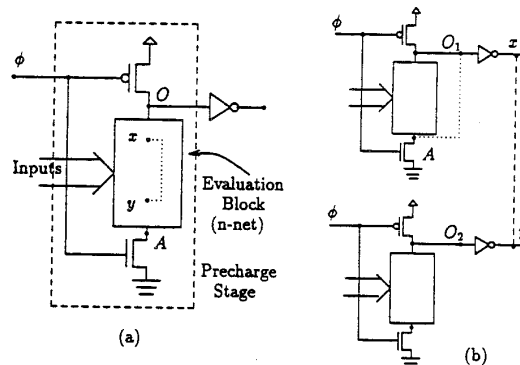


Figure 7: A domino logic gate

Another problem is due to the charge sharing effect at the precharge nodes. Again consider the circuit in Figure 7(a). If during  $\phi = 1$  there is no conducting path from  $O$  to  $A$ , then  $O$  is a floating node and should retain its logic value 1. However due to charge sharing between  $O$  and some nodes inside the evaluation block, the voltage value  $v$  at  $O$  may be less than  $VDD(5V)$ .

If  $v$  is larger than  $4V$ , no problem exists. If  $v$  is less than  $4V$  but larger than  $V_{DD}/2$ , due to the high noise immunity of CMOS circuits it is likely that the logic value at the output of the inverter is still at 0. Therefore logically no faults exist. Because of this when a designer designs a domino logic circuit, he may allow the resulting voltages at  $O$  after charge sharing to be at, say  $3.5V$ . This voltage will turn on both n- and p-type transistors and thus a larger current may exist in the inverter. Therefore the circuit may be identified as faulty if CSM is used.

Yet another problem is that the effect of one fault may be masked by the existence of another fault. Consider the circuit shown in Figure 7(b). To detect the fault  $(x, y)$ ,  $O_1$  and  $O_2$  must be set to complementary values. Assume we set  $O_1$  and  $O_2$  to 1 and 0 respectively. Due to another BF ( $O_1, A$ ), the value at  $O_1$  will be 0 during  $\phi = 1$  and thus no excess current exists.

In summary the release of A3 may result in the following problems: (1) many undetectable BFs may exist if only CSM is used; (2) a large current may flow through a gate driven by a floating node (or the precharge node); and (3) the detection of a single fault may be masked by the existence of other faults. These problems are not easy to eliminate. The undetectability of BFs in domino logic is an intrinsic problem due to the "precharge" property of these circuits, and appears to invalidate the use of CSM. The charge sharing problem may be alleviated by using a larger precharge node (in terms of capacitance). This, however, can result in performance degradation of the circuit. It seems that the fault masking problem always exists and cannot be avoided.

From the above discussions we can conclude that CSM is not an effective method for detecting BFs in domino logic.

## 4.2 Synchronous sequential circuits

In a sequential circuit, control loops always exist and thus A4 is always violated. Therefore CSM may fail for sequential circuits since nodes in a control loop may stabilize at incorrect logic values without consuming excess current. However to have this erroneous situation two conditions must be satisfied. First, there must exist no external control to the loop so that the logic values in the loop may change without consuming an excess steady state current. Second, the control loop must be a "real" loop, i.e., it must be a *logically active* loop, not just a *physical* loop. Consider the Huffman model of a sequential circuit shown in Figure 8(a). In the following discussion master-slave flip-flops are used as storage elements. Similar arguments can be applied to circuits using other types of storage elements. As shown in Figure 8(b) both the master and slave latches contain a control loop (indicated by dotted boxes). The control clock is shown in Figure 8(c). During  $CLK = 0$  the slave latch has an external control but not the master latch as explained next.

When  $CLK = 0$ ,  $u = v = 1$ . Thus control loop

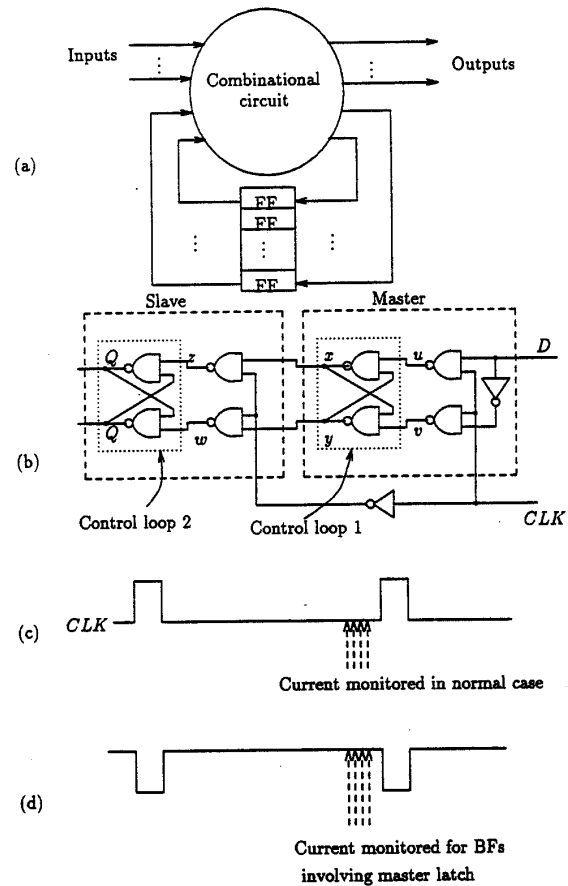


Figure 8: A sequential circuit with master-slave flip-flops

1 is not controlled by  $u$  or  $v$ , i.e., the value of  $x(y)$  may stabilize at either 1(0) or 0(1). Any BF to either  $x$  or  $y$  but not both can change the state of control loop 1 without consuming an excess current during steady state. For control loop 2 the situation is different. When  $CLK = 0$  one of  $z$  and  $w$  must have a logic value 0 and thus the control loop 2 is under the control of  $z$  or  $w$ . Thus the state of this loop cannot be changed without consuming an excess current.

If CSM is to be used for detect BFs in the combinational circuit (see Figure 8(a)), then the time to measure the current is near the end of the cycle when  $CLK = 0$  (when the circuit reaches its steady state) as indicated in Figure 8(c). At this time loop 2 is controlled by an external power source (i.e.,  $z$  or  $w$ ) but loop 1 is not. Therefore using CSM a bridging fault

between a node in loop 2 and another node in the combinational circuit, or between two nodes in loop 2, can be detected. A BF involving both  $x$  and  $y$  is also easy to detect since they are always complementary to each other. However a fault involving only one node in loop 1 may not be detected.

Two strategies can be used to deal with BFs involving only  $x$  or  $y$ . First, the possibility of having such BFs can be reduced by a careful layout. This can be done because both  $x$  and  $y$  are nodes within a FF. Another approach is by controlling the clock so that the clock waveform is as shown in Figure 8(d). One then can measure the current near the end of  $CLK = 1$ .

Note that due to the clock setting, the "global loops" (FFs—combinational circuit—FFs) do not logically exist during steady state. Thus BFs involving either  $x$  or  $y$  but not both are the only faults that may not be detected by CSM. This observation can be generalized to all synchronous sequential circuits since during steady state all global loops should not logically exist since otherwise races in the circuit will occur.

## 5 Conclusion

In this paper we have analyzed the applicability of IDDQ testing. In particular we have shown that any of the constraints proposed in [15] cannot be removed without causing problems. We have also given a detailed analysis on domino logic and synchronous sequential circuits. We have shown why IDDQ testing may not be effective for domino logic. For synchronous sequential circuits we have shown that only a few BFs cannot be detected by IDDQ testing and with a careful layout the probability of such faults can be reduced.

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