

Process Variations and their Impact on Circuit Operation ¹

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Abstract

The statistical variations in electrical parameters, such as transistor gain factors and interconnect resistances, due to variations in the manufacturing process are studied using data obtained from a 0.8 μm CMOS process. The impact of these variations and correlations on circuit operation is illustrated. Examples show that circuit delay can increase from the mean by about 100% due to crosstalk effects aggravated by process variations. Case studies emphasize the need for a tighter coupling between fabrication and circuit design and the need for new design corners based on process information.

1: Introduction

Modern digital VLSI designs employ gigahertz clock frequencies and deep submicron feature sizes. In such designs, the precision of the manufacturing process is extremely critical. A chip that has been designed disregarding effects of process variations is more likely to fail due to effects such as crosstalk ([1], [2], [3] and [4]), ground bounce ([5]), and delay.

To determine the extent of such effects, the distribution of various electrical parameters, such as device gain factors and interconnect resistances and capacitances, due to variations in the manufacturing process must be determined. Once this distribution is known, which is also called the design envelope, the design corners can then be identified. The importance of developing new validation strategies due to the presence of process aggravated noise (PAN) is discussed in [6]. In [7], the values of parameters of devices from 25 wafers are measured and used to perform statistical simulations which demonstrate that process variations can have a significant impact on circuit delay. In [8], models are developed to characterize the relationship between the values of device parameters (e.g., threshold voltage) and process parameters (e.g., dopant concentration). Also, in [9] existing tools are used to quantify the relationship between process parameters and delays of inverters. The objective of both these studies is to identify process parameters that most influence the device/circuit characteristics to enable better process control. An approach to build an accurate nonlinear

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model for mapping variations in process parameters to variations in a circuit performance parameter using additive regression splines is proposed in [10].

In this paper we present statistical distributions of the values of various electrical parameters and give examples to illustrate the effects of process variations on crosstalk and delay. The variations in the values of passive parameters, such as capacitances, are typically not considered during the validation of digital circuits [11]. Variations in the values of these parameters and their strong influence on circuit performance are brought to light. The importance of correlations between parameters in identifying realistic design corners is also demonstrated.

This project was carried out with wafer data obtained from the MOSIS service [12] of the Information Sciences Institute (ISI) of the University of Southern California. The data is from a 0.8 μm process with a single poly layer and three metal layers that uses 13 masks. The poly and diffusion are silicided and the process uses LDD technology.

2: Electrical Parameters

An array of AC and DC parametric test structures and a small number of functional test devices are provided on each die for monitoring the fabrication of wafers for the MOSIS service. Measurements on these test structures provide raw data, such as voltage and current values, from which one can compute the values of various electrical parameters. Good wafers are selected based on whether the measured values of certain parameters are within specified bounds.

The electrical parameters that are of interest to us are interconnect parameters, such as sheet resistances and line widths; device characteristics, such as threshold voltages and process gain factors; and inter-layer capacitances, such as area capacitances.

The work reported here is based on measurements made on a set of 15 wafer lots. The number of wafers in a wafer lot ranged from 3 to 10 with a total of 66 wafers in the population. Measurements were made on only 9 die on each wafer. The coordinates of these 9 locations are the same for each wafer in a lot, but may vary slightly over lots. Hence we have $9 \times 66 = 594$ measurements for any given parameter.

It should be noted that only values associated with good wafers are used in this study. Hence, all the values used lie between the upper and lower bounds as guaranteed by the manufacturer.

3: Analysis

Different types of analysis were performed to study the variation statistics of the parameters.

Histograms: For each parameter a histogram was plotted to observe the distribution of its values over the entire population. Also, for the single largest lot, histograms were obtained for each parameter for three cases: Case 1) for the entire wafer lot; Case 2) for data points at a particular die location across all wafers in the lot; and Case 3) for data points on all die on each wafer in the lot. A typical histogram is shown in Figure 1. This histogram corresponds to the sheet resistance of Metall1 as indicated by the acronym SR.

The x-axis of the histogram is normalized to percentage deviation from the mean. Statistics consisting of the mean, the standard deviation as a percentage of the mean, and the worst case deviation (max – min) as a percentage of the mean are indicated above the figure.

Sequence Plots: Since wafers within a lot are assumed to be manufactured at the same time, there is no chronological ordering among such wafers. A sequence plot for a parameter consists of a sequence of values of the parameter, where the values obtained from wafers within each lot are ordered in ascending order and those from different lots are ordered by the time of manufacture. Sequence plots were designed to identify any radical change in the parameter values and to locate anomalies. A typical sequence plot is shown in Figure 1. This sequence plot corresponds to the sheet resistance of Metal1.

Correlation Coefficients: A correlation coefficient was computed for each pair of parameters X and Y. The extreme values for this coefficient are +1 and –1. +1 signifies that the X and Y variations strictly increase or decrease together, and –1 signifies that the variations are in the opposite direction. Intermediate values signify varying degrees of correlation. A value of zero indicates no correlation, i.e., X and Y appear to be independent.

4: Results and Inferences

The results and inferences of the analysis for the individual parameter variations and the correlations are presented next.

Parameter variations: The individual parameter variations were estimated over the global population as well as for the largest wafer lot. These variations are presented in Table 1. Columns 3 through 5, respectively, show the mean, standard deviation as a percentage of the mean, and the worst case deviation (max – min) as a percentage of the mean. If the distribution of a parameter were normal, then its mean plus and minus twice (thrice) the standard deviation would cover 95.44% (99.74%) of the points. However, the distributions are not exactly normal. Hence, the percentage deviations on either side of the mean required to cover 98% and 95% of the data points in the respective distributions are calculated and tabulated in columns 7 and 8. The variations within the largest wafer lot are shown in column 6.

Inference on parameter variations: It was observed that transistor sizes do not have a significant impact on the threshold voltage variations. Poly sheet resistance variations are much higher than those in the diffusion sheet resistances which are in turn higher than those in metal sheet resistances. The large variations in the poly sheet resistance may be attributed to the varying degrees of resistivity induced by the siliciding process.

The relative variations of the values of parameters within the largest lot taken as a population follows the same pattern as the relative variations of the parameters in the global population. Also, for a given parameter, the variations over a lot are generally greater than the variations on each wafer which in turn are greater than the variations across wafers at a particular die location on the wafers. In other words, it has been observed that (variations in Case 1) > (variations in Case 3) > (variations in Case 2). One of the reviewers of this

paper suggested that variations within a die may be greater than the variations across a wafer, but we have no data on intra-die variations.

Correlations: The correlation coefficients between parameters are given in Table 2. The threshold voltages of the P and the N-channel transistors of the same size are found to be uncorrelated. The correlation coefficient between threshold voltages of minimum size (W:1.2 μ m, L:0.8 μ m) and wide (W:7.2 μ m, L:0.8 μ m) transistors were found to be 0.64, for both N and P-channel devices. The correlation coefficient between the gain factors of thin P and N-channel transistors was found to be 0.8 and between those of wide P and N-channel transistors was found to be 0.7. Sheet resistances were found to be highly correlated to the contact resistances that share a common layer with the sheet resistances. Area capacitances involving a common layer are also found to be highly correlated.

5: Impact of Process Variations on Circuit Operation

In this section we illustrate the effect of the variations in the values of electrical parameters due to process variations on circuit operation. The results are obtained by simulation using PSPICE, and values of individual electrical parameters used are within their acceptable bounds and are consistent with the correlations found and discussed in the previous sections.

In [13] analytical expressions are derived for crosstalk which help identify the device parameters whose values have a significant impact on crosstalk. In this work we study variations in and correlations between gain factors and threshold voltages as well as interconnect parameters. Variations in gate capacitances are ignored since in preliminary experiments they were found to have only marginal impact on circuit delay. Moreover, variations in the device gain factor also include the variations in the gate oxide capacitance, C_{ox} , since gain factor is $\mu \times C_{ox}$. Variations in body effect are ignored in this study since all devices in the circuits studied have zero drain-to-substrate voltages.

The above mentioned variations in and correlations between device and interconnect parameters were incorporated into existing SPICE models provided by MOSIS. This was easy for this set of parameters since each parameter in this particular set has corresponding parameters in the SPICE models. In general, due to the absence of an analytical technique, heuristics are used to map the variations in and correlations between the values of an arbitrary set of parameters into SPICE models.

Throughout this section any reference to extremum values that are chosen for a parameter always means the value of the parameter given by its *mean* * $(1 \pm y/100)$, where y is the percentage deviation on either side of the mean beyond which there remains 2% of the data points (see the column 7 of Table 1).

5.1: Example 1: Delay

The circuit used to study delay is shown in Figure 2. It consists of one inverter driving another inverter through an interconnect. The sizes of the transistors in the inverters and the length of the metal interconnect are chosen to obtain a realistic nominal driver output rise time of 130ps. (This is reasonable assuming a clock period of 4ns.)

First the case using the mean values for the electrical parameters is considered. Then, the maximum and minimum delay values that are obtainable through process variations are

calculated by choosing appropriate extremum values for individual parameters from their variation statistics that excite the worst case behavior. The delay is measured as $t_2 - t_1$, where $i(t_1) = z(t_2) = 2.5V$ (i.e., $0.5 \times$ power supply voltage). The delay values obtained are shown in Table 3. A variation of about 25% in the delay was observed. It was also observed that the delay is primarily influenced by the interconnect to substrate capacitance.

5.2: Example 2: Crosstalk Delay

To study the impact of crosstalk on signal delay we employed a circuit consisting of two sets of driver-load inverters whose interconnects are coupled through a mutual capacitance. One of the drivers is larger than the other, since it drives a longer line, and serves the purpose of inducing crosstalk in the other interconnect (see Figure 3). The delay of a signal arriving at the load of the weaker driver is influenced by the mutual capacitive coupling and by the type of transition that occurs at the stronger driver. This gives rise to three cases of delay due to crosstalk (refer to Figure 3):

1. C-1: 5V at i_1 ; falling transition at i_2 ,
2. C-2: rising transition at i_1 ; falling transition at i_2 ,
3. C-3: falling transitions at i_1 and i_2 .

Illustrative diagrams to show waveforms for cases C-2 and C-3 are shown in Figure 4. All delay values are measured as $t_2 - t_1$, where $i_2(t_1) = b(t_2) = 2.5V$. The nominal values of the delay are measured for each of the three cases mentioned above using the nominal values for all parameters. Then the worst case behaviors (max and min delay) are excited by using the appropriate extremum values for each parameter. The delay values obtained are shown in Table 3. The delay is found to vary by about 25% around its mean value. It can also be seen that the combined effect of crosstalk and process variation results in approximately 100% increase in the delay from its mean value (217.3ps to 400ps). Similar results are obtained even when a small amount of skew exists between the input transitions.

5.3: Example 3: Crosstalk Pulse Height

The circuit shown in Figure 3 was also used to study the variation in the crosstalk pulse height. A falling transition with fall time 100ps at the load of the stronger driver, while keeping the output of the weak driver charged at 5V, causes a pulse in the weaker line. The height of this pulse varies about a nominal value as the parameters of the circuit change due to process variations. The pulse height values obtained are shown in Table 4. The height of the pulse is found to vary by about 40% around its mean value.

5.4: Example 4: Effects of Correlations

The existence of correlations between electrical parameters is useful in discarding “fictitious” design corners that never occur in practice, and hence aid in identifying aggressive design styles and new design corners.

A simple example is used to demonstrate this fact. For the case discussed in Section 5.3, the height of the crosstalk pulse has been shown [3] to be proportional to K_{ns}/K_{pw} . If the height of the worst case crosstalk pulse is to be estimated, it is natural to assume the maximum possible value of K_{ns} and the minimum possible value of K_{pw} . From the

MOSIS data for the gain factors, the maximum value for K_{ns} is $6.2811 \times 10^{-5} A/V^2$ and the minimum value for K_{pw} is $1.3133 \times 10^{-5} A/V^2$. Hence, a design corner corresponding to $K_{ns}/K_{pw} = 4.783$ would be predicted. However, since K_{ns} and K_{pw} are highly correlated (Section 4), K_{ns} and K_{pw} increase or decrease together over die. Hence, the situation where K_{ns} is maximum and K_{pw} is minimum does not occur at the same die. In fact, the actual ratio of K_{ns}/K_{pw} is maximized for another pair of K_{ns} and K_{pw} values, namely, $5.7489 \times 10^{-5} A/V^2$ and $1.3861 \times 10^{-5} A/V^2$, respectively, obtained from the same die, resulting in a maximum value of 4.147. It should be noted that neither of the above two values are extremum. Hence, the new design corner now lies in the hitherto unexplored part of the design envelope.

6: Conclusion

Statistical analysis of the values of electrical parameters obtained by measurements on wafer lots of a $0.8 \mu\text{m}$ process shows significant variations of these parameters from their nominal values due to process variations. The variations in the values of many of these parameters are found to be correlated. The impact of these variations and correlations on circuit operation is demonstrated through four examples. It is shown that the variations that are typically ignored during circuit design may now be more significant due to their impact on the performance of a circuit. This necessitates a tighter coupling between the areas of fabrication and circuit design. Also, the knowledge of correlations between parameters is shown to facilitate the removal of fictitious design corners and identification of new design “corners”, thus enabling more aggressive designs. The results of this analysis point to new areas of concern to design, validation and test engineers.

Currently, a similar statistical analysis of data obtained from a $0.6 \mu\text{m}$ CMOS process is being performed. Initial results show that the percentage variations in the values of the inter-layer area capacitances and the device threshold voltages have increased with a reduction in the feature size, whereas those in the device gain factors and material sheet resistances have decreased.

7: Acknowledgment

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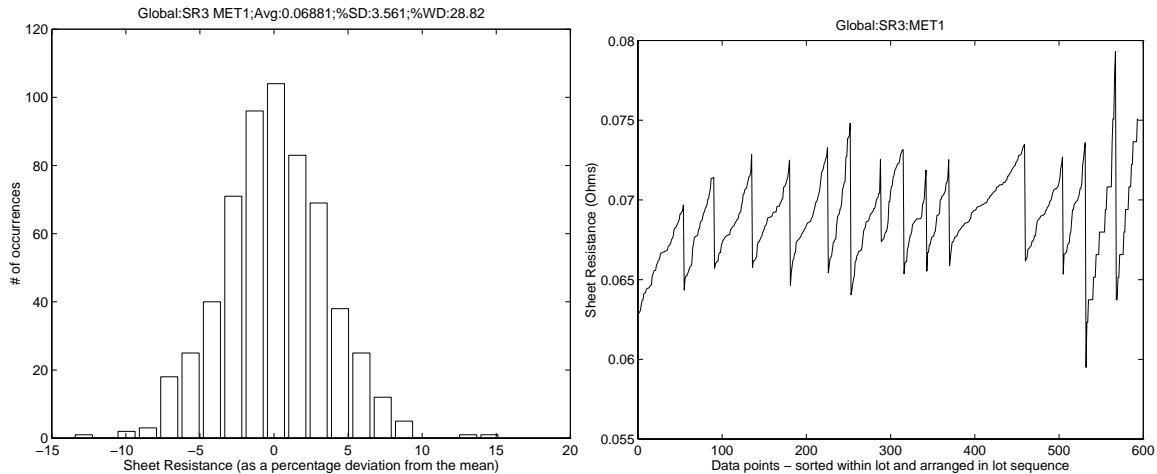


Figure 1. Histogram and sequence plot of Metal1 sheet resistance.

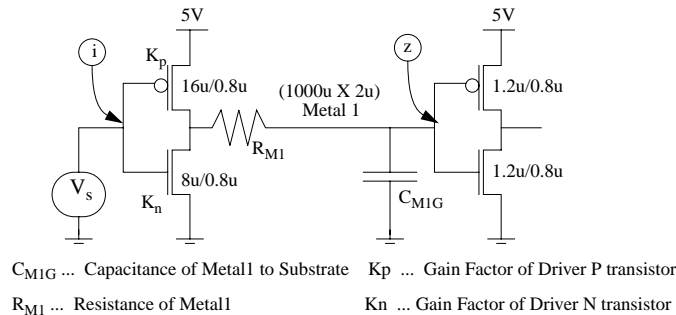


Figure 2. Experimental setup for simple delay.

Table 1. Parameter variations.

Electrical Parameters		Mean Value	% Std. Dev.	% Worst Case Dev.	Largest Lot % Worst Case Dev.	% Deviation from Mean covering x% of the points	
						x: 98%	x: 95%
Voltage Threshold	N:1.2/0.8	0.76 V	2.76%	15.7%	9.03%	6.29%	5.23%
	P:1.2/0.8	-0.91 V	2.35%	14.2%	9.53%	5.21%	4.26%
Gain Factor	N:1.2/0.8	$3.73 \times 10^{-5} A/V^2$	7.48%	38.8%	12.35%	15.51%	14.2%
	P:1.2/0.8	$9.04 \times 10^{-6} A/V^2$	6.67%	31.4%	16.39%	12.54%	11.49%
Sheet Resistance	P+ Diff	2.05 Ohms	6.41%	31.6%	18.1%	13.69%	12.63%
	Poly	2.08 Ohms	6.60%	46.3%	37.96%	16.99%	13.9%
	Metal1	0.07 Ohms	3.56%	28.8%	10.85%	8.64%	6.72%
Line Width	Metal1	3.76 μm	5.26%	29.3%	9.16%	10.75%	8.79%
	Metal2	3.61 μm	5.21%	20.1%	5.21%	9.38%	8.04%
Area Capacitance	Metal2 - Metal3	$3.2 \times 10^{-11} F/\mu m^2$	9.24%	41.9%	26.01%	19.55%	16.76%
	Poly - Metal2	$2.27 \times 10^{-11} F/\mu m^2$	6.34%	26.9%	16.10%	12.55%	11.66%
	Metal1 - Metal2	$3.03 \times 10^{-11} F/\mu m^2$	5.75%	30.0%	17.07%	13.0%	11.0%
	Metal1 - PWELL	$4.37 \times 10^{-11} F/\mu m^2$	6.46%	36.5%	3.18%	24.34%	8.52%
	Metal2 - PWELL	$2.34 \times 10^{-11} F/\mu m^2$	11.03%	55.2%	10.07%	29.46%	18.41%

Table 2. Parameter correlations.

Resistance Parameters		Contact Resistance		Sheet Resistance		
		P+ Diff - Metal1	Poly - Metal1	P+ Diff	N+ Diff	Poly
Contact Resistance	N+ Diff - Metal1	0.4	0.7	0.17	0.64	0.48
Resistance	Poly - Metal1	0.43	1.0	0.39	0.56	0.62
Sheet Resistance	P+ Diff	0.62	0.39	1.0	0.25	0.41

(a)

Area Capacitance	N+ Diff - PWELL	Poly - Metal1
N+Diff - Poly	-0.69	-0.79
N+Diff - PWELL	1.00	0.64

(b)

Area Capacitance	PWELL - Poly	PWELL - Metal3
PWELL - Metal2	0.73	0.76

(c)

Area Capacitance	Metal1 - Metal2	Metal2 - Metal3	Metal1 - Metal3
Poly - Metal2	0.88	-	-
Poly - Metal3	-	0.87	0.96
Metal1 - Metal3	0.82	0.87	1.00

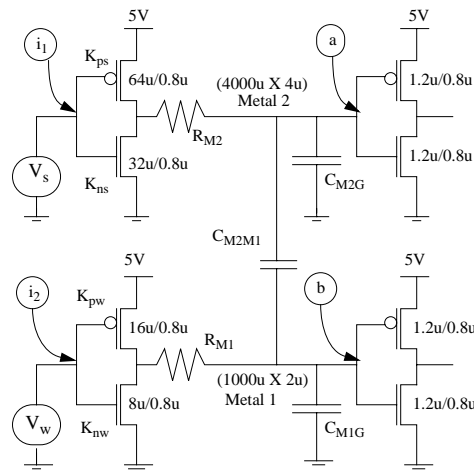
(d)

Table 3. Variations in delay.

Circuit Delay (T_d)		Mean Delay	Decreased Delay		Increased Delay	
		Value (ps)	Value (ps)	% Deviation from Mean	Value (ps)	% Deviation from Mean
Simple Delay		156.2	124.8	20.1	199.6	27.78
Crosstalk Delay	C-1	217.3	177.4	18.36	269.5	24.02
	C-2	315.0	248.0	21.27	400.0	26.98
	C-3	165.5	128.2	22.54	205.7	24.29

Table 4. Variations in crosstalk pulse height.

Circuit Parameter		Mean Height	Decreased Height		Increased Height	
		Value (V)	Value (V)	% Deviation from Mean	Value (V)	% Deviation from Mean
Pulse Height (H)		0.6465	0.4291	33.63	0.9333	44.36



C_{M1G} ... Capacitance between Metal1 and Gnd ; K_{ps} ... Gain Factor of strong driver P transistor
 C_{M2G} ... Capacitance between Metal2 and Gnd ; K_{ns} ... Gain Factor of strong driver N transistor
 C_{M1M2} ... Capacitance between Metal1 and Metal2 ; R_{M1} ... Resistance of Metal1
 K_{pw} ... Gain Factor of weak driver P transistor ; R_{M2} ... Resistance of Metal2
 K_{nw} ... Gain Factor of weak driver N transistor

Figure 3. Experimental setup for crosstalk effects.

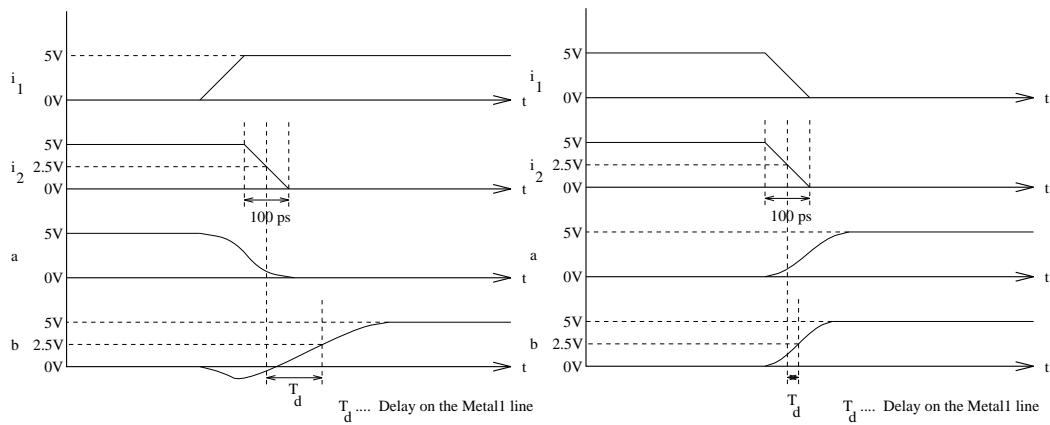


Figure 4. Waveforms for cases C-2 and C-3 of crosstalk delay.