

# Analytical Models for Crosstalk Excitation and Propagation in VLSI Circuits<sup>1</sup>

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## Abstract

We develop a general methodology to analyze crosstalk effects that are likely to cause errors in deep submicron high speed circuits. We focus on crosstalk due to capacitive coupling between a pair of lines. Closed form equations are derived that quantify the severity of these effects and describe qualitatively the dependence of these effects on the values of circuit parameters, the rise/fall times of the input transitions, and the skew between the transitions. For noise propagation, we present a new way for predicting the output waveform produced by an inverter due to a non-square wave pulse at its input. To expedite the computation of the response of a logic gate to an input pulse, we have developed a novel way of modeling such gates by an equivalent inverter. The results of our analysis provide conditions that must be satisfied by a sequence of vectors used for validation of designs as well as post-manufacturing testing of devices in the presence of significant crosstalk. We present data to demonstrate accuracy of our results, including example runs of a test generator that uses these results.

Index terms: crosstalk, pulses, delay, noise, test generation

## 1 Introduction

Advancements in the field of VLSI have lead to a decrease in device geometries (deep sub-micron technology), high device densities, high clock rates and thus small signal transition times. Thus, interconnection lines that were once considered to be electrically isolated can now interfere with each other and have an important impact on system performance and correctness.

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<sup>1</sup>This work was supported in part by the Semiconductor Research Corp. under contract No. 98-TJ-646, and by Intel Corporation.

One such interaction caused by parasitic coupling between wires is known as crosstalk. If not carefully considered during design validation, crosstalk can cause extra signal delay, logic hazards, and even circuit malfunction. Accurate modeling and simulation of interconnect delay due to crosstalk thus becomes increasingly important in the design of high performance integrated circuits.

The modeling and analysis of crosstalk between interconnection lines have previously received considerable attention. Most crosstalk transient analysis techniques model interconnects as microstrip lines and utilize the well known multiconductor transmission line theory [1]. The analysis of coupled lossy transmission lines has been considered by several researches [2]-[6]. Numerical methods to solve a model of lossy transmission lines in the time domain have been proposed in [7] and [8]. Simulation models for interconnects and crosstalk were reported in [9], [10]. Nonlinearity of the source and load networks, not addressed in these papers, were considered in [15]-[18]. Although the above techniques are very effective for specific cases, they provide little general (qualitative) insight into the coupling mechanism. In addition, these analysis methodologies are often not applicable to VLSI circuits because of the complexity of the circuit model used and resulting high computation time. Several recent researches have modeled capacitive crosstalk using distributed networks [46]-[54]. Some of the models proposed make special assumptions on circuit structures or rise/fall times, and several techniques are simulation-based and often require a pre-characterization process for each combination of aggressor/victim pairs. The above works mainly focus on accurate modeling of noise effects and may result in an excellent match between models and SPICE, but they lack insight on the dependence of noise effects on circuit and signal parameters. It is these insights that enable us to find the conditions that maximally excite and propagate the noise effect during automatic test pattern generation (ATPG), our target application. The analysis of crosstalk induced delay has also been considered in [47], [48], [52], [53], [55], and [56]. However, these approaches are based on static analysis without considering the input patterns that determine if logical isolation of aggressor and victim lines exists.

Although in [49] the authors have tried to address this issue, there is no timing information associated with their approach and hence a resulting "logical possible" excitation of both aggressors and victims may still be temporally impossible.

The motivation for the research associated with this paper deals with generating test patterns to stimulate large crosstalk effects in digital logic. This work is a radical extension of classical work on automatic test pattern generation (ATPG) [45]. Classical test generation procedures usually use a 5-valued algebra, such as 0,1,X, D and D\_bar, where D and D\_bar represent Boolean errors. To establish an error at a site (line) in a circuit that has a fault, such as a stuck-at zero, input patterns must be identified that would place a logic 1 at this site in the fault-free circuit. This is usually done in one of two ways. One technique is based on line justification, the second on backtracing and forward line implication. Once an error is established at the fault site, it is then propagated through the logic until it reaches an observable line. Test generators do not consider circuit delay, hence can be thought to employ a zero delay model. Thus, such test generators are independent of layout, technology scaling and device library, and hence tests can be generated early in the design cycle.

Some test generators employ a larger algebra, such as symbols for positive and negative pulses. These pulses are again considered relatively independent of actual circuit delays, and consist of a full voltage swing from one logic level to the other. The focus of our work is on crosstalk effects, such as pulses and signal speed-up and slow-down.

Signal transitions are modeled using two parameters, an arrival time and a transition time. We model a pulse very accurately based on its arrival time, initial transition time, height, width, and final transition time. Hence these quantities can be considered to be analog rather than digital signals. To implement such a value system, it is important to include the concept of signal and gate delay. Finally, to work within the ATPG framework, it is necessary to attempt to establish the desired signals at the target site at the appropriate time, and hence create a large crosstalk effect, and propagate the effect to an observable signal line. In addition, rather than just produce an output error, it is desirable to produce as large an effect as possible, hence such a test generation process is actually an optimization process, rather than a constraint satisfaction process. It is well known that ATPG is of exponential complexity and hence a major focus of research in this area deals with reducing run-time. For our system, we need to process complex signal, namely pulses and transitions, through a gate level model of a circuit. To accurately capture timing issues, test generation is carried out after layout, so inter-wire coupling capacitance, device drivers and load capacitance are all known. The focus of this paper is the development of the necessary circuit and gate level models needed to implement such a test generator for crosstalk effects. As an example, we are concerned with developing a fast and accurate way of propagating a pulse through a NAND gate, as well as how does the amount of skew between two transitions affect speedup and slowdown.

The research described in this paper was carried out to facilitate the development of a new ATPG of the type described above. This influenced our work in two main ways. First, we were interested in a qualitative understanding of the dependence of crosstalk pulse and delay excitation on circuit parameters and parameters of waveforms. Such understanding has significantly (albeit often intangibly) shaped the overall architecture of our new ATPG. Second, we were interested in obtaining models that quantify the severity of effects for a given circuit and a given sequence of two partially specified vectors. This computation may be performed tens of thousands of times during generation of tests for a single target. Hence, the run time complexity associated with using the derived relations need to be low, given that all sub-expressions dependent solely on circuit parameters are pre-computed. Also, these relations need to be computed for sequences of two partially specified vectors and under conditions where ranges (as opposed to fixed values) are known for timing and other parameters. Finally, the relations provide information required to consider tradeoffs that become necessary when worst-case conditions cannot be satisfied. For example, we were interested in relations that give the value of crosstalk delay for a range of skews between the transitions at affecting and victim lines and not merely for the skew that maximizes this quantity. This is due to the fact that our test generator cannot arbitrarily assign a worst-case skew at the crosstalk site, but must work with the (range of) skew value(s) given by the sequence of two (partially specified) vectors under consideration.

A methodology is presented and used to characterize cases where inputs to one or both coupled lines have transitions with arbitrary transition times, arrival times and directions. Our analysis starts with a model in the frequency domain ( $s$  domain) to obtain a closed form voltage transfer function. This is then transformed to obtain expressions in the time domain. These expressions are used to characterize the amplitude, width, energy, and timing of the pulse, as well as the speedup or slowdown of transitions due to crosstalk.

The paper is organized as follows. In section 2 crosstalk effects are described. In section 3 the proposed methodology to analyze crosstalk is presented, followed by the derivation of closed form expressions for the frequency

domain transfer functions and time domain signal waveforms. In section 4 we discuss the propagation of crosstalk noise. Finally, in section 5 we present our conclusions.

## 2 Crosstalk Effects and New Validation and Test Issues

### 2.1 Crosstalk Effects

In VLSI circuits it is very common to have wires running adjacent to one another. In submicron designs, due to the greater proximity of adjacent wires on the same layer, increase in the heights of wires (relative to their widths), and increase in the switching speeds of signals, the parasitic coupling effects are significant. Coupling effects produce interference between signals, referred to as crosstalk noise, and may increase or decrease signal delays and decrease signal integrity.

While parasitic coupling includes inductive and capacitive effects, in this paper we will restrict our attention to only capacitive effects. Crosstalk effects can lead to possible circuit malfunction (permanent errors) and increased power dissipation. Consider a positive pulse created on a victim line. If this pulse is applied to an input of a dynamic NAND gate and all other inputs of the evaluation logic are at logic value 1, then the output may be accidentally discharged. Since the charge lost cannot be restored in the evaluation phase, this leads to a degraded voltage at the gate's output. If the degradation is substantial it may lead to a logic error. Also a degraded voltage on a line can be regarded as a weak "1" that can increase the effective delay of a gate in the line's fanout. A crosstalk pulse can trigger an un-wanted PRESET of a flip-flop causing data to be lost and hence an error. Similarly, if a line with a large crosstalk pulse is connected to the clock input of the flip-flop, then this pulse can be interpreted as an additional clock pulse and cause the flip-flop to latch erroneous data. For the case of crosstalk delay effect, if a signal is late to arrive due to crosstalk and this signal is propagated along a path that has a small delay slack, then a flip-flop setup time violation can occur and cause an erroneous logic value to be latched in the flip-flop.

### 2.2 New Design Validation and Test Issues

In high speed circuits, signal integrity and timing are important issues for correct circuit operations. From the previous discussion, crosstalk can have a significant impact on signal integrity and delay and even result in erroneous circuit operation.

Due to the high complexity of crosstalk analysis, the development of a methodology to identify pairs (or, in general, sets) of lines where crosstalk noise is likely to exceed the noise margin or timing is essential to any practical validation methodology. In [30] it is shown that process variations also have a significant impact on the severity of crosstalk effects. Hence, parts of a circuit where crosstalk does not cause errors for nominal values of parameters can operate erroneously for other parameter values in the *design envelope*. The correctness of a design at all points in the design envelope is verified by validating the circuit at various *design corners*, i.e., extreme combinations of parameter values where the design is likely to fail. However, the design corners that are commonly used during validation do not represent the combination of parameter values where the severity of crosstalk is maximized [21]. In addition, the noise-

to-signal ratio tends to increase as feature sizes reduce. Hence validation for crosstalk noise is essential in designing high speed circuits.

Even if a design is found to fail at some extreme points in a design envelope, a circuit may not necessarily be redesigned, especially if redesign would make the attainment of some design objectives impossible or have an impact on a product’s schedule. In such a case, the resulting circuit will typically be guaranteed to operate at a vast majority of points within the design envelope, but not all. Thus, each manufactured device must be tested to ensure that it works correctly. Therefore we need to develop a test generation framework for crosstalk noise. Traditional logic level crosstalk fault models and PODEM based ATPG algorithms were presented in [39], [40], [41]. However, these models characterize crosstalk effects as static hazards having a full voltage swing, and result in an overestimation of noise. Since crosstalk is a finite energy transient effect, test vectors generated using these models may not be able to actually propagate the noise to POs or flip-flops because of the inertia inherent to gates. In [39], [40] the dependency of detectability on the propagation ability of the crosstalk signal has been shown, but the penetration depth computation assumes that all gates (and/or all kind of gates) have the same capability to impede crosstalk propagation. In reality, some paths tend to filter out crosstalk noise, while others are very hazard-sensitive depending on the analog properties of the gates. Due to the non-linearity of CMOS gates, crosstalk noise can be attenuated or amplified while propagating through a gate. Hence it is necessary to investigate the analog properties of CMOS gates to determine how crosstalk effects propagate. In addition, the above models ignore timing of signals, i.e., they consider zero signal rise/fall times and/or no gate delays. Since the amplitude of a crosstalk pulse depends on the affecting line switching speed and the crosstalk delay has a strong relationship with signal arrival times and rise/fall times (see section 3), it is necessary to consider analog properties and timing information of signals in the test generation process. Therefore the ability to *efficiently and accurately create a large crosstalk effect and propagate it with minimal attenuation* has not been previously addressed. Thus, it is important to develop models to analyze crosstalk effects, and integrate these models into a mixed-signal test generator for crosstalk noise. This paper deals with establishing the necessary framework for such a test generator. A subsequent paper will deal with the actual test generation system. Preliminary results on this work are described in [23], [30], [43], [44].

### 3 Crosstalk Model and Analysis

#### 3.1 Capacitive Crosstalk Model

To obtain insight into the nature of crosstalk and its qualitative dependence on the circuit parameters associated with the coupled lines, we use the lumped model of capacitive coupling shown in Fig. 1.

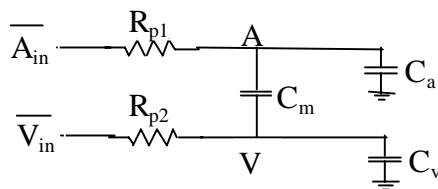


Fig. 1. Capacitive coupling model.

In this model, each pulling resistance,  $R_{p1}$  or  $R_{p2}$ , is composed of the line resistance and the on-channel resistance associated with the line driver. The load capacitances,  $C_a$  and  $C_v$ , consist of the line capacitance and the gate capacitance of the load driven by the line. Thus the line driver is equivalent to a pulling resistance, and the coupling network can be viewed as a network of capacitors ( $C_m$ ,  $C_a$ ,  $C_v$ ). Compared with the simplified model in [11], which assumed a linear rise/fall time on the node A (affecting line), our expanded model allows for a more general model of the signals  $A_{in}$  and  $V_{in}$ , not only in terms of their switching rates but also their relative skew. It also produces sufficient accuracy for our test generation application.

### 3.2 Driver Modeling and Approximation of Distributed RC Network Using Lump Models

Using the lumped model in Fig. 1 one can derive analytical expressions for crosstalk waveforms. However, as interconnect lengths increase, the error introduced by the lumped model increases. Hence two enhancements are made to (1) model the driver considering the rise time of the input signal, and (2) account for the distributed nature of the interconnect RC network. Item (2) is handled using a model for the effective coupling and load capacitance. Once this is done, the accuracy of this model approaches the accuracy of a distributed model, but the resulting analytical equations are nearly as simple as for a lumped model. These enhancements were made based on the results in [31].

### 3.3 Analytical Equations from Crosstalk Waveforms

We de-couple the system shown in Fig. 1 into an input waveform stage, a driver characterization stage and a coupling network stage. By doing this, we can employ more complex models to obtain more accurate results, take into account input waveforms other than ideal step functions, and thus analyze crosstalk induced speedup and slowdown (delay).

By using Laplace transformations, we can accomplish the following:

- 1) for the input waveform stage, obtain the Laplace transfer expressions for fairly complex inputs;
- 2) for the driver characterization stage, obtain the transfer function of the line driver model at a desired degree of accuracy;
- 3) for the cross-coupling network, obtain the transfer function from A to V.

By cascading these three stages we can obtain an expression for crosstalk in the s-domain that can be transformed back into the time domain. The analytic response derived is based on the first order model of MOS device behavior, commonly referred as the LEVEL 1 model, assuming that the channel modulation is negligible. This model was selected because more sophisticated models that take into account higher order effects are intractable for analytic manipulation. The insights gained from the results obtained using this simple model are sufficiently useful for our applications.

#### 3.3.1 Analysis of Crosstalk Pulse

To illustrate the analysis procedure, consider the case of a positive crosstalk pulse induced on node V (victim line) due to a rising transition at node A (affecting line). The input  $A_{in}$  to the inverter driving the affecting line is a

falling transition, and the input  $V_{in}$  to the inverter driving the victim line is kept high so that the victim line should remain at a constant low. The values for coupling capacitance and load capacitance can be obtained by techniques mentioned in section 3.2.

After the input to  $A_{in}$  is applied, the pulling device (PMOS) of the inverter driven by  $A_{in}$  can be modeled by its on channel resistance,  $R_{on}$ , connecting A to  $V_{DD}$ ; the corresponding NMOS device is off. The inverter driven by  $V_{in}$  can be modeled by the channel resistance of its NMOS device connecting V to GND. For computational convenience, we normalize  $V_{DD}$  to be 1 and GND to be 0. Fig. 2(a) shows the circuit model for the situation just described. Fig. 2(b) shows an equivalent circuit of Fig. 2(a).

Some notation used throughout the rest of this paper is described next:

A - node or signal on line A,

$A(t)$  - voltage at A in time domain,

$A(s)$  - voltage at A in frequency domain,

$A_{exp}(t)$  - voltage at A when  $A_{in}(t)$  is an exponential signal and  $V_{in}(t)$  is stable at low or high,

$A_{step}(t)$  - voltage at A when  $A_{in}(t)$  is a step function and  $V_{in}(t)$  is stable at low or high,

$A_{su}(t)$  - voltage at A when  $A_{in}$  and  $V_{in}$  are exponential inputs with identical directions of transition (speedup),

$A_{sd}(t)$  - voltage at A when  $A_{in}$  and  $V_{in}$  are exponential inputs with opposite directions of transition (slowdown).

In the above, A and V can be interchanged to obtain another set of notation.

Let “H” indicate a transfer function and its subscript indicates a node name or the conventional output/input notation.

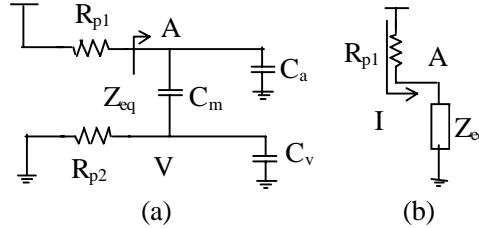


Fig. 2. Circuit model for crosstalk pulse analysis: (a) circuit model for a positive pulse induced on V due to a rising transition on A; (b) an equivalent circuit.

For a step input, we get

$$V(s) = H_V = \frac{C_m}{R_{p1}C_t} \left( \frac{1}{w-u} \right) \left( \frac{1}{s-w} - \frac{1}{s-u} \right), \quad \text{and} \quad A(s) = H_A = \frac{1}{s} - \frac{1}{w-u} \left( \frac{1}{s-w} - \frac{1}{s-u} \right) \left( s + \frac{C_m + C_a}{R_{p2}C_t} \right),$$

where w, u are solutions to the quadratic equation,  $s^2 + s \left( \frac{R_{p1}(C_m + C_a) + R_{p2}(C_m + C_v)}{R_{p1}R_{p2}C_t} \right) + \frac{1}{R_{p1}R_{p2}C_t} = 0$ , and both w and u are negative.

The time domain voltage waveform  $V(t)$  is obtained by taking the inverse Laplace transformation of its corresponding s-domain expression, resulting in  $V(t) = \left( \frac{C_m}{R_{p1}C_t} \right) \left( \frac{1}{w-u} \right) (e^{wt} - e^{ut})$ .

For arbitrary input waveforms instead of a step function, we can modify the transform for the input waveform. For example, assume the input to the driver stage is an exponential rising waveform with known transition time (time constant). The output transition time (time constant  $x$ ) of the output waveform  $(1 - e^{-t/x})$  for the driver is obtained using the output transition time prediction technique described in [31]. The corresponding victim line time domain response is

$$V(t) = \frac{C_m}{R_{p1}C_t} \left( \frac{1/x}{(w + 1/x)(w - u)} e^{wt} + \frac{1/x}{(u + 1/x)(u - w)} e^{ut} + \frac{1/x}{(w + 1/x)(u + 1/x)} e^{-t/x} \right)$$

Finding the maximum amplitude of the pulse can be done by differentiating the above equation and setting the result to zero. However, the above equation contains three exponential terms and it is very difficult to find a closed-form expression for the amplitude. Hence we expand the exponential terms by using the Taylor series expansion technique. The most important process in the Taylor series expansion is finding the expansion center,  $t_0$ , where the approximation error is minimal. Since we know that the time when the maximum amplitude of the pulse at  $V$  occurs will be near the time when the affecting line finishes its transition, one can set  $t_0$  to that value.

By expanding the expression for the crosstalk pulse into a Taylor series, a polynomial equation is obtained that can be solved directly to find the time ( $t_x$ ) when the maximum amplitude occurs. Then the maximum crosstalk amplitude is obtained by substituting  $t_x$  back into the crosstalk pulse equation. The derivation of the crosstalk amplitude expression is very lengthy and is omitted here. The approximation error in estimating the amplitude using this technique is less than 3%.

By using sensitivity analysis on these equations, we can observe that the severity of crosstalk is directly proportional to the mutual capacitance, resistance of line  $V$ , and inversely proportional to the resistance of line  $A$ , signal transition time, and the load capacitance on each line.

### 3.3.2 Analysis of Crosstalk Delay

By using the techniques described above we can analyze effects such as (1) when both signals  $A$  and  $V$  change simultaneously and in the same direction to cause signal speedup, (2) change in opposite directions to cause extra delay, and (3) change with a relative timing skew.

Consider the case where line  $A$  has a falling transition and line  $V$  has a rising transition. The equivalent circuit model is shown in Fig. 3. Here we assume that exponential waveforms of time constants  $x$  and  $y$  are applied to  $\overline{A}_{in}$  and  $\overline{V}_{in}$ , respectively, and the  $A_{in}$  signal has a time skew of  $z$  units with respect to signal  $V_{in}$ , where  $z$  can be positive or negative.

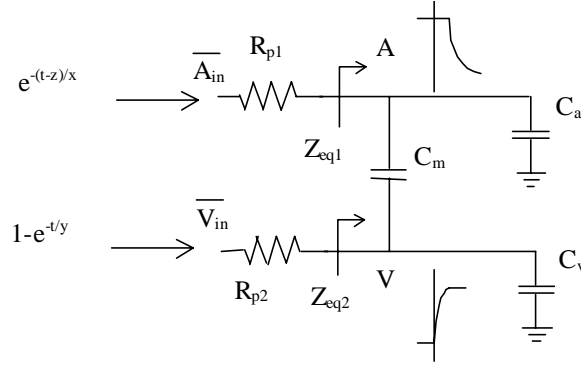


Fig. 3. Equivalent circuit for crosstalk delay analysis.

By using the techniques described in the previous section, the Laplace transformation for shifting the time-axis, and proper initial conditions, we have the following results.

The waveforms for A and V are given by the expressions

$$A_{sd}(t) = A_{exp}(t) + \frac{1}{y} \left[ \frac{c}{(w+1/y)(w-u)} e^{wt} + \frac{c}{(u+1/y)(u-w)} e^{ut} + \frac{c}{(w+1/y)(u+1/y)} e^{-t/y} \right],$$

$$V_{sd}(t) = V_{exp}(t) - \left[ \frac{1}{x} \left[ \frac{b}{(w+1/x)(w-u)} e^{w(t-z)} + \frac{b}{(u+1/x)(u-w)} e^{u(t-z)} + \frac{b}{(w+1/x)(u+1/x)} e^{-\frac{(t-z)}{x}} \right] U(t-z) \right],$$

where

$$A_{exp}(t) = \left\{ \frac{1}{x} \left[ \frac{w+a}{(w+1/x)(w-u)} e^{w(t-z)} + \frac{u+a}{(u+1/x)(u-w)} e^{u(t-z)} + \frac{a-1/x}{(w+1/x)(u+1/x)} e^{-\frac{(t-z)}{x}} \right] + e^{-\frac{(t-z)}{x}} \right\} U(t-z) + U(t) - U(t-z),$$

$$V_{exp}(t) = 1 - e^{-t/y} - \frac{1}{y} \left[ \frac{w+f}{(w+1/y)(w-u)} e^{wt} + \frac{u+f}{(u+1/y)(u-w)} e^{ut} + \frac{f-1/y}{(w+1/y)(u+1/y)} e^{-t/y} \right],$$

$$a = \frac{C_m + C_a}{R_{p2} C_t}, \quad c = \frac{C_m}{R_{p2} C_t}, \quad b = \frac{C_m}{R_{p1} C_t}, \quad f = \frac{C_m + C_v}{R_{p1} C_t}, \quad C_t = C_m C_v + C_m C_a + C_a C_v,$$

and  $U(t)$  is a unit step function.

The terms in  $A_{sd}(t)$ , except for  $A_{exp}(t)$ , contribute to the slowdown effect caused by the mutual capacitance. The terms in  $V_{sd}(t)$  contribute in a similar way.

Similar equations have been derived for speedup [23].

Fig. 4 shows the amount of speedup or slowdown due to coupling effects, assuming that the input signals switch simultaneously, i.e.,  $z = 0$ . The circuit configuration consists of two unbalanced drivers with a 4000 $\mu\text{m}$  long and 4 $\mu\text{m}$  wide metal2 affecting line A driven by the larger driver (32 $\mu\text{m}/0.35\mu\text{m}$  PMOS and 16 $\mu\text{m}/0.35\mu\text{m}$  NMOS), and a 1000 $\mu\text{m}$  long and 2 $\mu\text{m}$  wide metal1 victim line V driven by the smaller driver (8 $\mu\text{m}/0.35\mu\text{m}$  PMOS and 4 $\mu\text{m}/0.35\mu\text{m}$  NMOS). R, C and gain values used for analysis and simulations have been extracted from a layout.

Consider the case where V has a rising transition and A remains constant. Then from the curve labeled  $V_{exp}(t)$  in Fig. 4(a) we see that V reaches  $V_{DD}/2 = 1.65$  volts at about  $t = 77\text{ps}$ . Now if A simultaneously has a rising transition (see  $V_{su}(t)$ ), then V reaches 1.65 volts at  $t = 54\text{ps}$ , i.e., 23ps earlier. This illustrates the concept of crosstalk speedup.

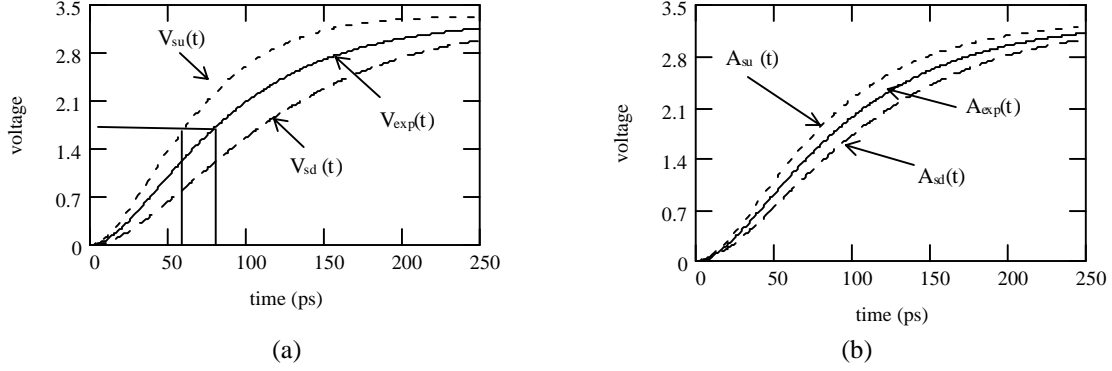


Fig. 4. Crosstalk speedup and slowdown effects assuming simultaneously switching inputs where both inputs have a transition time of 200ps. (a) effects on victim line; (b) effects on affecting line.

### 3.4 Dependence of Crosstalk Effects on Input Transition Times and Skews

In this section we investigate in more detail the dependence of crosstalk on input transition times and skew.

#### 3.4.1 Crosstalk Delay

Let the delay between the transition at the input of a line's driver and that at the line's far end for a falling transition at the line be  $t_d$  when the other line is static,  $t_{d-su}$  when both lines have transitions in the same direction, and  $t_{d-sd}$  when both lines have transitions in opposite directions. The speedup-time due to the coupling effect is  $(t_d - t_{d-su})$ , and the slowdown-time is  $(t_{d-sd} - t_d)$ . Fig. 5 shows the effects of slowdown with respect to input waveform switching rates, i.e., the time constants  $x$  and  $y$  of the exponential inputs. For simplicity, again we assume both signals switch simultaneously. As  $x$  decreases, the exponential waveforms  $e^{-t/x}$  and  $(1 - e^{-t/x})$  approach ideal step functions. In CMOS technology used here the signal rise/fall times range from 50ps to 300ps, thus  $x$  ranges from 22 to 130. The curve labeled  $y = 22$  corresponds to the case when the victim line input  $V_{in}$  has a rise time of 50ps; the one labeled  $y = .01$  corresponds to a step function.

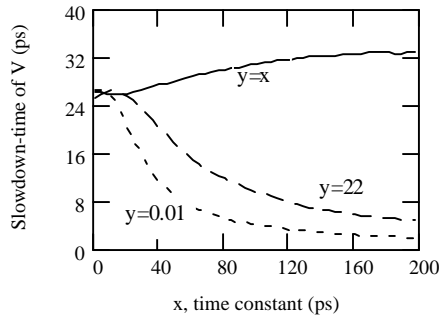


Fig. 5. The victim line slowdown-time vs. input switching rates.

From Fig. 5 we can see that when the input signal to the victim line is kept at a fixed switching rate, then the faster the affecting line changes the larger the slowdown of the victim line. Also for the case  $x=y$ , we see that the absolute amount of slowdown increases as  $x$  increases. For example, an exponential signal with a rise/fall time of 50ps ( $x = 21.7$ ,  $t_d = 39$ ps) has a slowdown-time of 26ps and one with a rise/fall time of 200ps ( $x = 83.33$ ,  $t_d = 108$ ps) has a

slowdown-time of 30ps. However, the percentage change in delay decreases as both  $x$  and  $y$  increase. The slowdown-time in the former case (50ps) represents a 67% increase in delay, while that in the later case represents a 28% increase in delay. This implies that slow transition signals have a smaller effect than fast transition signals.

Similar results have been obtained for the case of speedup [23].

We now consider the amount of speedup and/or slowdown as a function of the time skew  $z$ , when  $A_{in}$  and  $V_{in}$  have rise/fall time of 100ps.

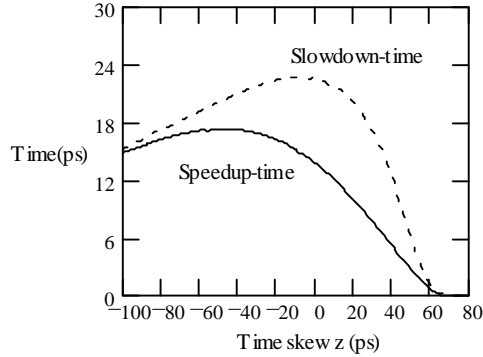


Fig. 6. Victim line speedup-time and slowdown-time vs. skew  $z$ .

From Fig. 6 we observe that as  $z$  increases (from  $-\infty$ ) the amount of speedup and slowdown on  $V$  first increases and then decreases. For the speedup situation, if  $A$  switches from low to high (high to low) earlier than  $V$ , then  $A$  helps charge (discharge)  $V$  before  $V$  changes, increasing the speedup. The amount of speedup reaches its maximum value when the coupling effect from  $A$  is maximum i.e., where the pulse at  $V$  due to  $A$  is maximum. After that, the remaining effect of  $A$  on  $V$  starts to dissipate and hence the speedup decreases. Also we can observe that for our example the slowdown is maximum when the signals switch simultaneously. This can be explained by considering the fact that a rapid change in the voltage at  $A$  transfers charge to node  $V$  via the coupling capacitance  $C_m$ . If the transition at  $V$  occurs concurrently with the transition at  $A$ , then the entire charge transferred is discharged via the pull down of the inverter driving line  $V$ , increasing its fall time. On the other hand, if  $A$  switches earlier than  $V$ , then some of the transferred charge is discharged via the pull up of the inverter driving the line  $V$  prior to its switching. Hence only a part of the charge transferred from  $A$  is discharged when  $V$  begins to fall, decreasing the slowdown. If  $A$  switches later than  $V$ , then for a time  $z$ ,  $V$  transits toward its target value before  $A$  affects it, hence the slowdown is decreased. For  $z$  greater than some fixed amount  $z_0$ ,  $A$  cannot impact  $V$  since  $V$  has already reached 50% of  $V_{DD}$ , which defines the delay time  $t_d$ . As the driver ratio increases (decreases), the skew for the maximum slowdown to occur also increases (decrease). In the technology being discussed, a single inverter delay is around 70ps. Hence the skew  $z$  can be within 2 or 3 gate delays and still have a significant effect.

### 3.5 Test Vector Generation

The results of our analysis provide conditions that must be satisfied by a sequence of vectors used for validation of designs as well as post-manufacturing testing of devices in the presence of significant crosstalk. Fig. 7 shows an example of test pattern generation for a crosstalk pulse. Assuming that we want to create a positive pulse at  $V$ , at least a

or b must be set to 1 to provide a constant low at V. However, we know from our analytic expressions that the height of the pulse is proportional to the victim line's driver resistance, i.e., to increase the total pulling resistance to GND, only input a is set to 1. Since a sharp transition on A is preferred (pulse strength is inversely proportional to the signal transition), both c and d are assigned rising transitions. In addition to the pulse excitation, to propagate the resulting pulse through the next stages, proper values must be set on side fan-in's of each gate, i.e. values for e, f, g must be set accordingly. Backward implication of these conditions will give rise to a sequence of test patterns.

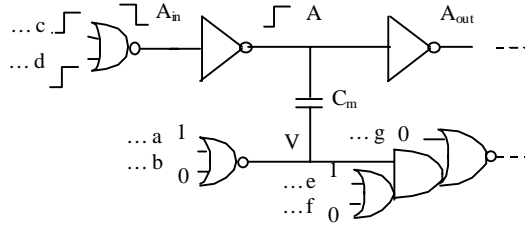


Fig. 7. Example circuit for test vector generation.

## 4 Noise Propagation

To accurately propagate noise through gates, we need to (1) characterize the noise waveform, (2) construct gate transfer functions, and (3) compute output noise waveforms. Since many CMOS gates in a random logic circuit have different electrical characteristics, our approach is to first model CMOS logic gates as equivalent inverters and then calculate the output response of noise through this gate using the transfer function of the equivalent inverter. In Section 4.1 a new inverter model is presented that reduces the error found in other approaches caused by neglecting the short circuit current. In Section 4.2 we propose a method to specify an inverter that is equivalent to a given CMOS logic gate (NAND, NOR) in terms of propagating noise effects. In section 4.3 we characterize the noise waveform and calculate the propagated output noise waveform through the equivalent inverter. So, unlike classical ATPG systems that use a universal mapping function between the inputs and outputs of a gate, our mapping functions are technology dependent and must be derived once of each library element.

### 4.1 A New Inverter Model

Several analytic models have been proposed for the transient response of CMOS inverters [13], [14], [25], [26]. Although these models take into account the influence of the input waveform on the propagation delay, the short-circuit current is neglected. Since crosstalk noise is a finite energy transient phenomenon, we propose an improved model for a CMOS inverter that takes into account the short-circuit current so that the error in estimating the propagated noise can be significantly reduced.

Consider the CMOS inverter in Fig. 8(a). We wish to determine the falling output waveform  $V_o(t)$  due to a rising input ramp  $V_{in}(t)$  with rise time  $t_r$ . Assume all circuit capacitance is lumped into one grounded load capacitance C

at the inverter's output and all voltages have been normalized with respect to  $V_{DD}$ . The charging of the capacitance  $C$  can be expressed by

$$I_p = -I_n - I_c = -I_n - C \frac{dV_o}{dt}.$$

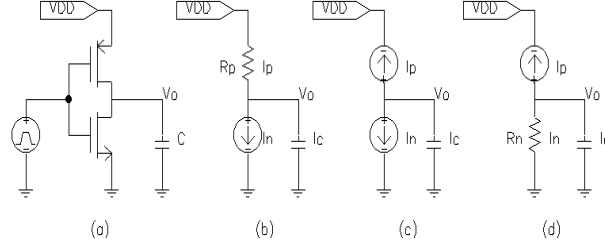


Fig. 8. CMOS inverter and its corresponding model when N and P MOS transistors operate in different modes: (a) circuit, (b) PMOS in linear and NMOS in saturation mode, (c) both in saturation mode, and (d) NMOS in linear and PMOS in saturation mode.

When the input is first applied, the NMOS (PMOS) is in the saturation (linear) region and can be modeled as shown in Fig. 8(b), where we replace the NMOS by a current source and the PMOS by a resistance. As long as the PMOS is in the linear region, the circuit can be characterized by the differential equation

$$\frac{1 - V_o}{R_p} = C \frac{dV_o}{dt} + \frac{\beta_n V_{DD}}{2} (V_{in} - v_{tn})^2.$$

Here  $\beta_n$  ( $\beta_p$ ) is the gain factor, and  $v_{tn}$  ( $v_{tp}$ ) is the transistor threshold voltage normalized with respect to  $V_{DD}$  of the NMOS (PMOS) transistor.

With the initial condition  $V_o = 1$  when  $V_{in} = v_{tn}$ , integration yields

$$V_o = P \cdot e^{-\frac{(t-t_r v_{tn})}{R_p C}} + A(V_{in} - v_{tn})^2 + B(V_{in} - v_{tn}) + D, \quad (1)$$

where  $K = \beta_n V_{DD} / 2C$ ,  $P = 2R_p^3 C^3 K / t_r^2$ ,  $A = -R_p CK$ ,  $B = 2R_p^2 C^2 K / t_r$ , and  $D = 1 - 2R_p^3 C^3 K / t_r^2$ .

However, the on-channel resistance  $R_p$  of the PMOS transistor in this model is not constant during the input transition.  $R_p$  is small (P-channel is fully ON) when the input is small and becomes very large when the PMOS transistor saturates to become a current source. Taking this non-constant property into account we modify the channel resistance as a function of input waveform, namely, we set

$$R_p = \frac{1}{\left| \beta_p V_{DD} (V_{in} - 1 - v_{tp}) \right|},$$

where  $V_{in}(t) = t/t_r$ .

When the input is rising and the output voltage drops to  $(V_{in} - v_{tp})$ , the PMOS transistor goes into saturation. The circuit can now be modeled as shown in Fig. 8(c) and can be described by the equation

$$\frac{\beta_p V_{DD}}{2} (V_{in} - 1 - v_{tp})^2 = \frac{\beta_n V_{DD}}{2} (V_{in} - v_{tn})^2 + C \frac{dV_o}{dt}.$$

Integrating the above equation we obtain

$$V_o = \frac{\beta_p V_{DD} t_r}{6C} (V_{in} - I - v_{tp})^3 - \frac{\beta_n V_{DD} t_r}{6C} (V_{in} - v_{tn})^3 + M, \quad (2)$$

where  $M$  is a constant and can be obtained by using the boundary condition ( $V_o = V_{in} - v_{tp}$ ) in both equations (1) and (2).

As the output voltage continues to drop, the NMOS transistor will eventually operate in the linear region. The circuit can now be modeled as shown in Fig. 8(d). The equations characterizing this region are similar to the case in Fig. 8(b).

Fig. 9 shows the result of our new model. The input waveform is assumed to be a ramp having a rise time of 250ps, and the load capacitance is 15fF. We use a rise time of 250ps because, as shown in [30], when an affecting line has a transition with a 100ps rise time, the slope of the rising edge of the crosstalk noise on the victim line is about 250ps. The results using our model match SPICE results very well except for the tail portion of the response. Note that the result based on ignoring the PMOS transistor has a significant error. We have carried out this analysis for two different technologies and many different signal transition times and consistently obtain very accurate results.

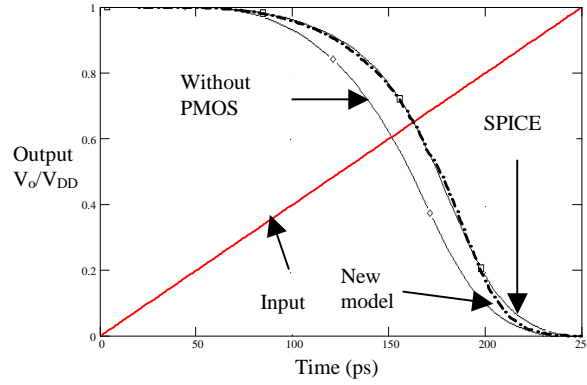


Fig. 9. Comparison of analytic result of proposed model and SPICE simulations.

## 4.2 A Method to Collapse CMOS Gates

Our approach for computing the output noise for a general CMOS gate is to collapse the gate to an equivalent inverter and then apply the results in Section 4.1. We set the side fan-in's to their non-controlling values. Collapsing techniques have previously been used for computing propagation delay [26], [27], [28], [29]. The methods presented in [26] treat series transistors as series resistors and adds the widths of parallel devices. This leads to an inaccurate estimate of delay. Although the approach in [29] provides a good estimation of propagation delay, the predicted output waveforms do not match well with SPICE simulations. Since the propagation of noise depends heavily on the gate's response, we have developed a new but simple approach to collapse CMOS gates into equivalent inverters.

### 4.2.1 Series MOS

The effective transconductance,  $\beta_{\text{eff}}$ , of  $n$  series-connected transistors is traditionally approximated as  $\beta/n$ . This approximation is valid only when the input is a step function, all transistors operate in their linear regions. Consider the

pull-down NMOS chain of a CMOS NAND gate in Fig. 10(b), where the  $V_{DS}$  and/or  $V_{GS}$  of each MOSFET in the series-connected chain is smaller than that of the inverter (Fig. 10(a)). Assume that all devices have identical  $\beta$  values and that there are no more than 5 MOSFETs connected in series. When the input transition is applied, the switching MOS first operates in the saturation mode and then moves into the linear region. In addition, during the first part of the input transition all transistors above the switching MOSFET operate in saturation and those below the switching MOSFET operate in the linear region. This results in the primary source of error in the use of the  $\beta/n$  approximation. Thus, to take this artifact into account, we need to estimate  $\beta_{\text{eff}}$  under various conditions of operations.

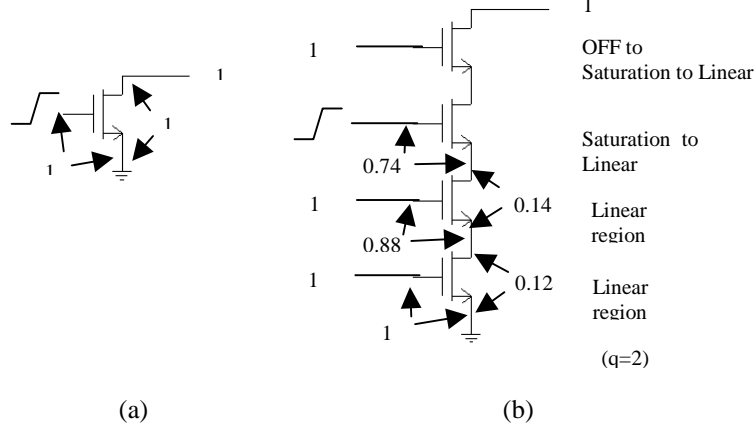


Fig. 10. Pull-Down NMOS chains; (a) single MOS, (b) series connected MOS, all values normalized w.r.t.  $V_{DD}$ .

When the input transition first occurs, both the MOS in Fig. 10(a) and the switching MOS in Fig. 10(b) are in the saturation region and thus  $V_{GS}$  determines the device current. For the single MOS in Fig. 10(a), assume  $V_{GS} = v_{\text{inv}}$  is the input voltage at which  $V_{\text{out}} = 0.5$ , i.e.,  $V_{DD}/2$ . For the switching MOS in Fig. 10(b) to conduct the same amount of current so that  $V_{\text{out}}$  can drop to  $V_{DD}/2 + \sum_i V_{DS}^i$ , the input voltage applied to the switching device must be  $v_{\text{inv}} + \sum_i V_{DS}^i$ , where  $i$  ranges over all  $q$  transistors below the switching MOS. At the instant that the switching MOS moves from the saturation region into the linear region, the voltages across the  $q$  MOSFETs below the switching device are as indicated in Fig. 10(b). Hence the summation term is approximately equal to  $0.14 \times q$ , and the estimated input voltage is  $(v_{\text{inv}} + 0.14 \times q)$ .

Therefore when the switching MOS is in the saturation region and the PMOS transistor with its own effective  $\beta_p$  is in the linear region,

$$\beta_{\text{eff}} \cong \beta \left[ \frac{V_{\text{inv}}}{(v_{\text{inv}} + 0.14 \times q)} \right] = \beta_1.$$

As  $V_{\text{out}}$  continues to drop, the PMOS transistor in the pull-up network will go into its saturation region and change its effective  $\beta_p$ . To deal with this situation, one can either modify the effective  $\beta_p$  directly or continue to modify the  $\beta_{\text{eff}}$  of the pull-down network to compensate for the change in  $\beta_p$ . We chose the later approach because we can use interpolation to easily approximate the modification for  $\beta_{\text{eff}}$ .

Before developing the interpolation approach, consider the next region where the switching MOS goes into the linear region. Here the MOS can be modeled as an on-channel resistor except that its  $V_{DS}$  is not the whole output voltage drop and the devices above the switching MOS will move into the linear region one by one. Hence instead of using the traditional  $\beta_{eff}$  value of  $\beta/n$ , a correction term is needed. The effective transconductance when a switching MOS is in the linear region is approximated by  $\beta_{eff} = \beta_2 = m \frac{\beta}{n}$  where  $m$  is a constant determined empirically. We have found that  $m = 0.75$  works well when the number of devices below the switching MOS range from 0 to 5, which is usually the case for a NAND gate.

Returning to the region where both the complementary PMOS and the switching MOS are in the saturation region, by interpolation from the other two cases presented, we get

$$\beta_{eff} = \beta \left[ \left( \frac{V_{DD} - V_{in}}{V_{DD} - v_{inv}} \right) \left( \frac{\beta_1 - \beta_2}{\beta} \right) + \frac{m}{n} \right].$$

Because the above approximation involves the input  $V_{in}$  which makes it difficult to find a closed-form solution,  $\beta_{eff}$  can be further approximated by  $\beta_{eff} = \alpha \beta_1 + (1 - \alpha) \beta_2$ , where  $\alpha$  is an empirical constant. We have found that  $\alpha = 1/3$  works well when the number of devices below the switching MOS range from 0 to 5. The accuracy of this approach heavily depends on the  $\beta_{eff}$  value, which is a function of technology dependent fitting coefficients such as  $m$  and  $\alpha$ .

#### 4.2.2 Parallel MOS

When propagating noise through a CMOS gate, since all side fan-in's have to be set to their non-controlling values, the parallel network is reduced to a single transistor whose gate is connected to the switching input.

#### 4.2.3 Internal Capacitance

Internal capacitances are usually ignored when they are small compared to the load capacitance. The easiest way to take into account the effects of internal capacitance is to add it to the load capacitance, but this results in an overestimation of the propagation delay and output transition time. Hence our approach is to model MOS devices as ON-channel resistances and use the Elmore delay model to obtain the equivalent load capacitance at the gate output.

Consider the pull-down NMOS chain shown in Fig. 11(a). Since the transistor M2 is ON before the input is applied to the switching device (M1), the internal capacitance  $C_{p2}$  is completely discharged. Also M0 is ON so  $C_{p1}$  is charged. When the input is applied, all transistors are turned ON and hence can be modeled by their linear resistance as shown in Fig. 11(b).

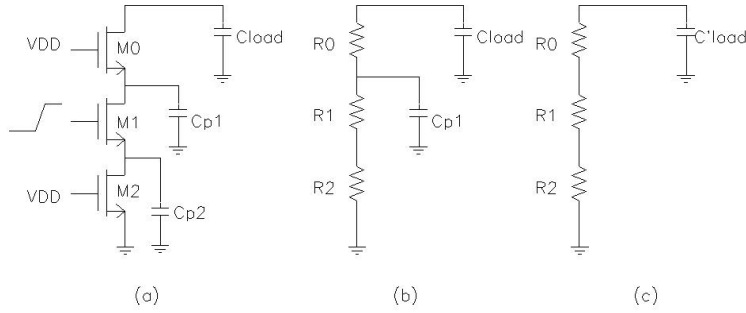


Fig. 11. (a) Pull-down subcircuit of a NAND gate, (b) corresponding RC model to obtain lumped load capacitance including internal capacitance, and (c) the circuit with all capacitance lumped into the load capacitance.

Using the Elmore delay model, the time constant for the circuit in Fig. 11(b) is  $C_{p1}(R_1+R_2)+C_{load}(R_0+R_1+R_2)$ , or equivalently  $C'_{load}(R_0+R_1+R_2)$ , where  $C'_{load} = C_{p1} \frac{R_1 + R_2}{R_0 + R_1 + R_2} + C_{load}$ .

Fig. 12 shows an example circuit for comparing the results from SPICE simulation and the collapsing technique. The input is a ramp having a rise time of 100ps and the load is 20fF. All device sizes are (4u/0.8u) and we assume all capacitances are lumped into the output load. The dash curve is the output waveform of the equivalent inverter obtained using the collapsing technique, and the solid curve was obtained by SPICE simulation.

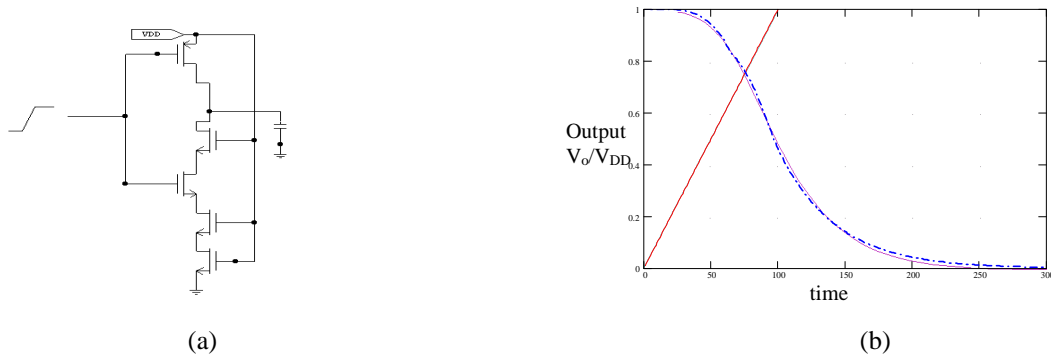


Fig. 12. (a) Circuit for collapsing NAND gate into an equivalent inverter, (b) model and SPICE simulation results.

#### 4.2.4 Multiple Input Transitions

Computing  $t_r$  (or  $t_f$ ) for the equivalent inverter is complicated when more than one input to a gate switches. First we apply the method in Section 4.2.3 to lump all internal capacitances to the output load. That is, all  $C_p$ 's below the lowest switching MOSFET are discharged to "0" and, depending on the current state of the circuit, either all other internal  $C_p$ 's or only those above the highest switching MOSFET are added to the output load. Then we use the techniques in [29] to find the equivalent input.

Percentage errors of the proposed collapsing model (model v.s. SPICE) are shown in Table 1 for rise/fall times and Table 2 for 50%-50% delay time. The circuit configuration is similar to the one in Section 4.2.2. From the analysis in Section 3, crosstalk noise diminishes rapidly as the rise/fall time of input signals increase. Hence we try to minimize the estimation error of rise/fall times due to gate collapsing when fitting the technology coefficients for effective  $\beta$ . A good example of the fitting is the NAND4 case (Fig. 12) when the switching input is at the second position from the output, where we have a 0.93% error in the fall time and 3.25% in the delay time. However, due to the limitation of the use of square-law I-V models, our technique has its limitations in matching the whole waveform exactly. Since the minimization has been performed for the rise/fall time, we see larger percentage errors in Table 2.

One can also observe that there are large percentage errors when multiple (all) inputs are switching. Beside the fact that multiple input switching is still one major concern for CMOS macro-modeling, one other reason is that the Miller coupling from the gate to the output has not been modeled in our technique. This coupling will cause the output to have an overshoot and push the whole waveform later to introduce additional delay. This effect is more severe when multiple inputs are switching at the same time with short rise/fall times. For our application the accuracy of our model is sufficient. In fact, this accuracy is usually less than the changes created by process variations.

Table 1 Percentage rise/fall time error using the collapsing method.

Gate type	Input position (1st = closest to output)				
	1st	2nd	3rd	4th	All switch
NAND2	0.76	1.52	-	-	4.54
NAND3	2.4	3.66	1.39	-	11.54
NAND4	-1.2	-0.93	-0.61	2.35	15.29
NOR2	8.1	8.9	-	-	10.7
NOR3	-2.6	-0.9	-8.47	-	-1.69
NOR4	-7.6	-9.2	-8.26	-5.54	-3.22
NOT	2.6	-	-	-	2.6

Table 2 Percentage delay error using the collapsing method.

Gate type	Input position (1st = closest to output)				
	1st	2nd	3rd	4th	All switch
NAND2	5.33	6.94	-	-	-19.4
NAND3	8.33	10.8	9.9	-	-22.72
NAND4	8.04	3.25	5.44	-7.3	-34.1
NOR2	10.52	3.57	-	-	-16
NOR3	8.62	6.25	-3.22	-	-25.8
NOR4	9.1	-2.3	-7.3	-11.4	-32.86
NOT	4	-	-	-	4

### 4.3 A Piece-Wise Linear Model for Noise

When a crosstalk noise (a pulse) passes through a gate, it can be either attenuated or amplified depending on its amplitude  $H$  and width  $W$ . Fig. 13 shows a simulation result of crosstalk noise propagating through an inverter. In Fig. 13(a) the output noise is small. On the other hand, the input noise in Fig. 13(b) is sufficient to produce a large output pulse. Note that the output reaches its minimum after the amplitude of the input noise starts to decrease. In addition, the output pulse is almost symmetric with respect to  $t_q$ , the time it reaches its minimum value.

There are two obvious ways to obtain the output waveform as a function of the input waveform. The first is to use the crosstalk waveform equations developed in Section 3 convolved with the equations described in Section 4.1. The second is to use a piece-wise linear model of the input noise and approximate the output response using the transformation developed in the previous sub-sections. The latter technique is preferred because it is reasonable accurate and computationally efficient. Let the value of the input voltage be  $H'$  when the output reaches its minimum. There are two instants of time where the input has the value  $H'$ , labeled  $t_p$  and  $t_q$  in Fig. 13(b). We approximate the input pulse waveform by three linear segments, as shown in Fig. 13, namely

- 1) a rising ramp from the start of the noise until the input reaches the value  $H'$  at time  $t_p$ ,
- 2) a constant value of  $H'$ , and
- 3) a falling ramp from  $H'$  at time  $t_q$  and going through the point where the input voltage drops to  $V_{th}$ .

Assume  $H'$  is a linear function of  $H$ , i.e.,  $H' = \rho H$  for  $0 \leq \rho \leq 1$ . Experimental results show that when  $H$  is in the range of 1-3.3V,  $\rho$  is in the range from 0.85-0.87. By using the crosstalk pulse equations derived in the previous section, the slope and time period of each segment can be easily determined. We can apply this piece-wise linear approximation of the noise waveform to the inverter model described in section 4.1 to obtain the output response.

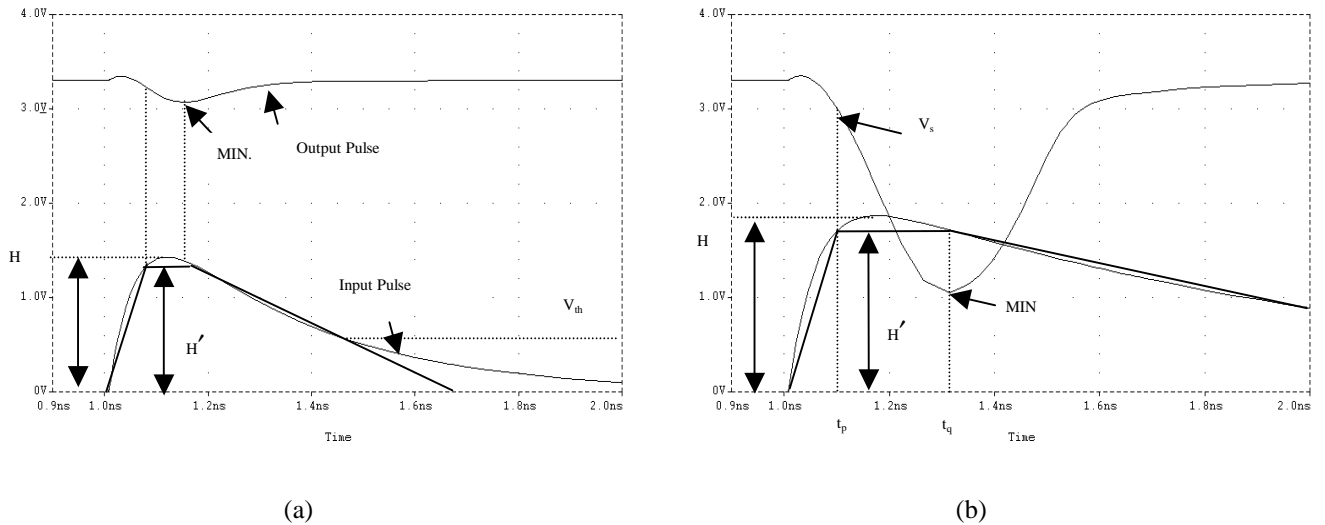


Fig. 13. Crosstalk pulse passes through an inverter (a) a small input pulse, (b) a large input pulse.

To complete our model we need to set a critical voltage  $v_x$  such that a pulse with amplitude less than  $v_x$  will be attenuated and one larger than  $v_x$  will be amplified. This critical voltage  $v_x$  can be defined as the input voltage such that  $dV_{out}/dV_{in} = -1$ . Since this point resides in the region that is modeled by the circuit in Fig. 8(b), the following results are obtained from equation (1).

$$\frac{dV_{out}}{dV_{in}} = P \cdot e^{-\frac{t_r(V_{in}-v_m)}{R_p C}} \cdot \frac{-t_r}{R_p C} + A(V_{in} - v_m) + B = -1. \quad (3)$$

Solving for  $V_{in}$  we obtain the critical voltage  $v_x$ . An approximate value of  $v_x$  can be found by using a Taylor series expansion for the exponential term.

If  $H$  is smaller than  $v_x$ , the circuit model in Fig. 8(b) is used to determine the output response. First we apply the first segment of the noise waveform, i.e. the rising ramp, to the model in section 4.1 and obtain the output voltage drop to  $V_s$  at time  $t_p$  as shown in Fig. 13(b). Then the second segment, a level voltage of value  $H'$  is applied that continues to discharge the output. Similar to the process in Section 4.1, except the input is now held constant at  $H'$ , we obtain the output response as

$$V_{out} = P e^{-t/R_p C} + M R_p C, \quad t_p < t \leq t_q, \quad (4)$$

where  $R_p = \frac{1}{V_{DD} \beta_p (H' - 1 - v_{tp}) \text{Coef1}}$ ,

$$P = e^{-t_p/R_p C} (V_s - M R_p C),$$

$$M = \frac{1}{R_p C} - \frac{V_{DD} \beta_n}{2C} (H' - v_m)^2,$$

and Coef1 is an experimental fitting coefficient and is a function of  $H$ .

The minimum output voltage obtained is  $V_{out}(t_q)$ .

For values of  $V_{in} > v_x$ , a change,  $dV_{in}$ , in the input voltage will cause a change,  $dV_o$ , in the output voltage such that  $dV_o$  will be greater than  $dV_{in}$ , i.e. the circuit is in the amplification mode. The circuit model in Fig. 8(c) is used to determine the output response. Similar to the above process for the case of a small pulse, we obtain the output response

$$\text{as } V_{out} = Z \cdot t + (V_s - Z \cdot t_p), \quad t_p < t \leq t_q, \quad \text{where } Z = \left[ \frac{\beta_p V_{DD}}{2C} (H' - 1 - v_{tp})^2 - \frac{\beta_n V_{DD}}{2C} (H' - v_m)^2 \right].$$

Again the minimum output voltage is  $V_{out}(t_q)$ .

If the output voltage continues to drop, the NMOS transistor will pull out of saturation and move into the linear region, and the inverter will no longer operate in the amplification mode. The circuit model in Fig. 8(d) is then used to calculate the output response. The resulting equations for the output response are similar to equation (3), except the roles of the NMOS and the PMOS transistors are interchanged and the coefficients are different. Again the corresponding minimum output voltage is  $V_{out}(t_q)$ .

After the output reaches its minimum voltage, the third segment of the model, the falling ramp, is applied to the inverter model to obtain the recovery portion of the output waveform. This is the reverse of the previous processes in obtaining the discharging waveform. However, since we already observed that the output waveform is almost symmetric around  $t_q$ , another approach to obtain the recovery portion of the output waveform is just to reflect the discharging part of the waveform with respect to the axis  $t_q$ . The error caused by this “reflection” method is mainly in the tail portion of the output waveform. Since the variance in the tail portion is less than the device threshold voltage ( $v_{in}$  or  $v_{tp}$ ), this approximation has a negligible effect on the results.

Propagation of this output pulse through the next level of gates is done in a similar way. Fig. 14 shows a comparison of this approach with SPICE results. The figure compares the amplitudes of pulses at lines OUT1 and OUT2 obtained via SPICE simulation with those obtained by using the proposed model, for seven different crosstalk pulse heights. We show the comparison only for voltages around the critical voltage  $v_x \approx 1.745V$ , because for other voltages, SPICE and our model are in complete agreement. Here we see that for an input height equal to about  $v_x - 0.15V$ , the pulse at OUT1 is about 0.7V and is essentially zero at OUT2. For an input of about  $v_x + 0.05V = V^*$ , the pulse at OUT1 is more than  $V^*$ , and that at OUT2 is almost 3V.

For crosstalk speedup and slowdown the piece-wise linear model can be easily constructed by using the arrival and transition times of the signal.

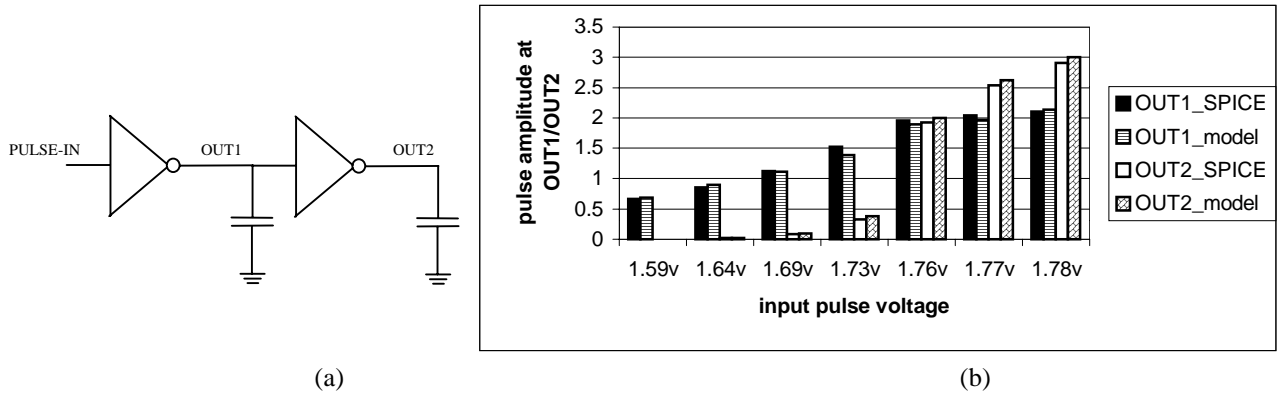


Fig. 14. (a) Circuit for measurement for input and output pulses amplitude  $H'$ ; (b) Comparison of the model and SPICE results.

Combining all the techniques described in Section 4.1 – 4.3, i.e., the inverter model, the method to collapse CMOS gates and the piece-wise-linear model, Fig. 15 shows the results of applying input pulses to the middle input of a 3 input NAND gate. The other two inputs are held at “1”. Fig. 15 shows only the amplitude (actually,  $H'$ ) for the resulting pulses, the other parameters such as  $t_a$ ,  $t_p$ ,  $t_q$ , and  $t_e$  are within 10% of the values produced by SPICE. Note that the accuracy is most significant at voltages close to  $v_x$ , since otherwise the pulse is either attenuated or amplified significantly.

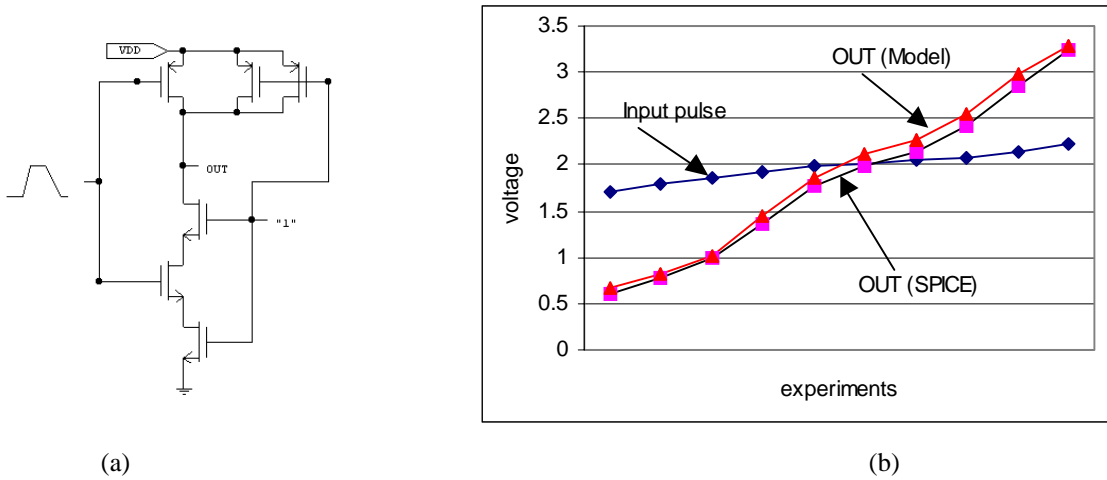


Fig. 15. (a) Circuit for applying piece-wise-linear pulses; (b) Comparison of the model and SPICE results (maximum pulse amplitudes).

The following example shows the results applying the above models and our ATPG algorithm to the example circuit shown in Fig. 16. The channel lengths of all devices are 0.35um and under each gate we indicate the ratio of the widths of the PMOS to NMOS FETs. The gain factor ratio of the NMOS to PMOS in the technology file used is 3.8. All wire and gate capacitances correspond to a realistic layout. Gate sizes are computed to achieve signal transition times of 100ps. Primary inputs are assumed to have signal transition times of 100ps.

Assume that the sub-circuit on the left side of the dash line is 1000um apart from the sub-circuit on the right side of the dash line. Hence lines 14, 9 and 13 are assumed to be about 1000um long and 4 um wide. In addition, assume that line 13 is the affecting line in metal1, line 9 is the affected line in metal2, and they overlap so that there is a significant coupling between them. The gate driving line 13 is assumed to be a buffer which has a strong driving strength.

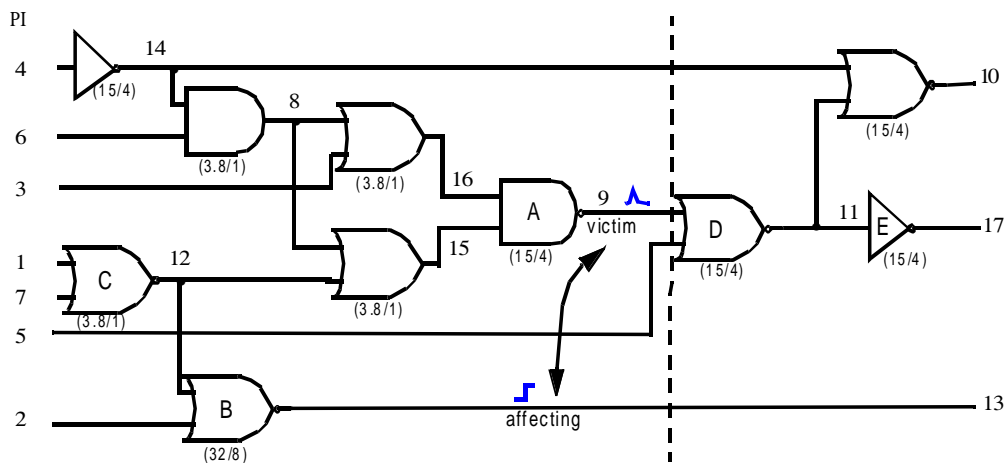


Fig. 16. Example circuit to illustrate the algorithm.

Assume that we would like to create a positive crosstalk pulse on the victim line 9. First we attempt to set a 0 on this line. Since gate A is a NAND gate, all its inputs have to be set to “1”. By backtracing a possible PI assignment setting PI3 to 1, PI6 to 1, and PI4 to 0 is found. Next we attempt to create a rising transition on the affecting line. PI2 is selected first and set to a falling transition. According to our analytical result, a fast transition is preferred for creating a larger noise. For having a fast transition on the affecting line, the preferred side fan-in’s of gate B are “0”. Hence, either PI1 or PI7 is set to 1.

By our equations the affecting line starts to transit at time 45ps with a rise time of 62ps. We calculate the crosstalk noise waveform (strength) according to equations in section 3. The crosstalk noise has an amplitude of 1.62V with the peak time at 95ps. To propagate this noise, the propagation path has to be sensitized and hence PI5 is set to “0”. Since the path through the gate driving line 10 is blocked by the assignment of PI4 to 0, the only observation point is line 17. The noise at line 11 has an amplitude of 1.19V and the inverter attenuates this pulse so that no significant noise is obtained at the PO line 17. The comparison of the model result and SPICE is shown in Table 3 and demonstrate the accuracy of our models. The fact that the pulse could not be propagated to an output is not surprising because of the nature of the 0.35um technology and the static gates used in the example. In SCMOS 0.35um technology the dielectric material between metal 1 and metal 2 is still thick enough so that the coupling capacitance is not sufficiently large to create a severe crosstalk problem. In addition, static gates are usually well balanced for pull-up and pull-down capability which in turn weakens the noise, unless the noise is very large.

Another experiment was performed to see whether the noise is worse for dynamic logic. Gate D was replaced by a dynamic gate with a minimum-size weak keeper. This dynamic gate is very sensitive to noise. The results are shown in Table 4 where we see that significant noise is created at the primary output. Once again this table illustrates the accuracy of our models.

Table 3 Comparison of the model and SPICE results.

Parameter	Noise site (line 9)			Line 11			Primary output (line 17)		
	Noise amplitude	Peak time	Start time	Noise amplitude	Peak time	Start time	Noise amplitude	Peak time	Start time
Model	1.62	95	45	1.19	143	71	0	-	-
SPICE	1.64	100	42	1.17	150	78	0	-	-

Table 4 Comparison of the model and SPICE results for circuit with dynamic gate D.

Parameter	Noise site (line 9)			Line 11			Primary output (line 17)		
	Noise amplitude	Peak time	Start time	Noise amplitude	Peak time	Start time	Noise amplitude	Peak time	Start time
Model	1.62	95	45	2.40	162	70	3.24	241	120
SPICE	1.64	100	42	2.42	170	76	3.20	250	125

## 5 Conclusion

We have presented a methodology to analyze crosstalk that provides closed-form approximations for pulse and delays generated by crosstalk as well as those that capture their propagation via circuit gates. Accuracies and complexities of these expressions are shown to be suitable for the intended applications, namely CAD tools for test generation for crosstalk.

The derived closed-form expressions show that the severity of crosstalk pulse is directly proportional to the coupling capacitance and the ratio of the strengths of the drivers driving the affecting and victim lines, and inversely proportional to the signal transition time and load capacitance on each line. In addition to similar relationships, for crosstalk slowdown the expressions also show that the slowdown is significant only for a range of skew values around zero. These qualitative insights have been used to define the architecture of our tool that identifies crosstalk effects that should be considered for validation and test generation. They have also shaped the architecture of our ATPG for crosstalk [43], [44].

The derived expressions are also used in the above tools because they provide desirable level of accuracy at low complexity. (In ATPG, the sub-expressions that depend only on circuit parameters are pre-computed to reduce run-time complexity when analyzing millions of candidate vector pairs.)

In [30] we show that crosstalk effects are significantly aggravated by variations in the fabrication process. The significance of the process variations necessitates the identification of new design corners for validation. For 0.18 $\mu$ m technology and beyond, the aspect ratio of, and spacing between, wires are such that the capacitance between metal wires on the same layer exceeds the interlayer capacitance. Since there is a high likelihood of having long parallel wires on the same layer, crosstalk effects become more severe.

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