

Test Generation for Ground Bounce in Internal Logic Circuitry*

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Abstract

Ground bounce in internal circuitry is becoming an important design validation and test issue. In this paper a new circuit model for ground bounce in internal circuitry is proposed. Based on this model an algorithm for generating test patterns that maximize ground bounce in combinational logic is presented. Our algorithm is also applicable to other test problems such as delay testing in the presence of excessive ground bounce.

1. Introduction

Signal and power integrity are crucial problems in VLSI systems. Modern trends in deep sub-micron circuit designs, such as high operating frequencies, short rise/fall times, and lower supply voltage, exacerbate this problem. For years, noise has been an important issue in board design. More recently, noise internal to a chip has become an important issue. This noise is due to several factors such as crosstalk, ringing and ground bounce. Ground bounce, also known as simultaneous switching noise (SSN) or delta-I noise, is a voltage glitch induced at power/ground (P/G) distribution connections due to switching currents passing through either wire/substrate inductance or package lead inductance associated with power or ground rails. This effect occurs not only because of switching in input/output (I/O) drivers, but also in internal circuits [1], [9]. One common method to deal with ground bounce in internal circuitry is to limit the noise magnitude. Designers are often given a noise budget, such as 10% of power supply voltage. After finishing a design, they perform some simulations based on estimated switch-

ing activities and local P/G networks to check if the ground bounce is over budget. If it is, the design is modified to accommodate this requirement using one of several techniques, such as adding de-coupling capacitances [4], [9]. Not all design techniques are effective in solving this problem [1]. Moreover, process variations in deep sub-micron technology lead to variations in electrical parameters and SPICE-like simulation of circuits may not correctly capture this effect. Hence, ground bounce in internal circuits has become a new design validation and test problem.

In Section 2, ground bounce problems in internal circuitry and its test approaches are described. In Section 3, a new model of internal circuitry for ground bounce, and its analysis, are presented. In Section 4, a cost function is determined based on the proposed circuit model. An algorithm for generating tests for maximum ground bounce in fan-out free circuits is presented in Section 5. In Section 6 and 7, circuits with/without re-convergent fan-out are discussed and the necessary modifications to the proposed algorithm given in Section 5 are described. Conclusion and future research area are summarized in Section 8.

2. Ground bounce problems and test

Ground bounce in internal logic is becoming an increasingly more serious problem. For ground bounce to cause errors, some electrical and logic conditions must be satisfied. The example in [1] is re-visited and shown in Figure 1. To cause an error in the output Z, the gate to source voltage of transistor M1 should be greater than its threshold voltage. If the ground bounce at node V_g due to noise in its ground circuitry and the ground bounce at node Y due to its virtual ground are in phase, M1 may not turn on and no error will occur. If they are somewhat out of phase, then M1 may turn on. Also, as shown in the figure, the value at line Z should be logic 1 for an error to occur. Some other conditions mentioned in [7] regarding crosstalk can be applied to ground bounce as well. For example, a large ground bounce coupled to a set/reset line may erroneously set/reset a flip-flop. In general, the test

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approach for this ground bounce, as shown in Figure 2, is as follows.

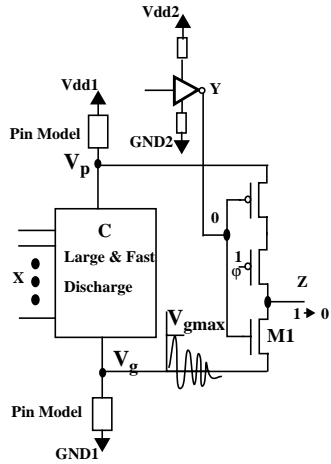


Figure 1. A generic example of how ground bounce causes errors in internal logic.

- 1) Identify the target site - some design styles have less noise tolerance than others, and some portions of a circuit may generate larger ground bounce than others.
- 2) Satisfy electrical and logic conditions and apply inputs to produce ground bounce - based on conditions required to cause an error at the target sites, test sequences are determined to excite the errors.
- 3) Propagate the errors to primary outputs or observable registers - the propagation methods used in stuck-at fault testing can be applied here.

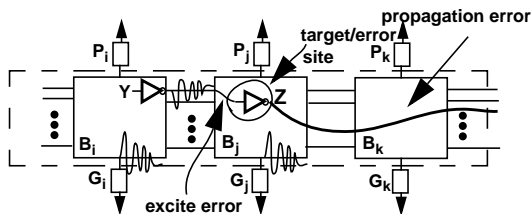


Figure 2. Generate tests for detection of likely logic errors.

Another problem of concern, as shown in Figure 3, is the effect of ground bounce on delay. Ground bounce will increase/decrease gate delays depending on the phase difference between the virtual ground and the input signals. The increase in gate delay under excessive ground bounce may affect the critical delay path selection because some non-critical paths, where ground bounce is ignored, may, in presence of ground bounce, have longer delay than what were considered to be critical paths. The test approach for

this problem is to generate tests that both (1) excite significant ground bounce as well as (2) test for critical delay paths in the presence of ground bounce.

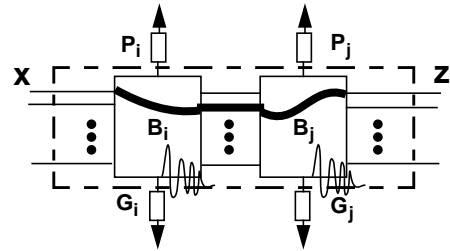


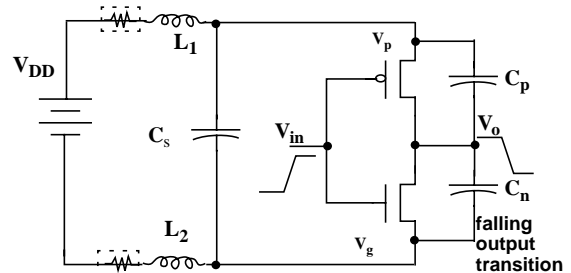
Figure 3. Generate tests that excite worst case delay in presence of significant ground bounce.

For the problems mentioned, one important issue that must be addressed is identifying an input sequence that produce the target ground bounce. That will be the main focus of this paper.

3. Model for ground bounce in internal circuits

3.1 Circuit model

Many circuit models dealing with I/O buffers and P/G networks have been studied [2-6]. These models include



- C_s - substrate and on-chip decoupling capacitances
- C_p is P-type and C_n is N-type parasitic capacitance
- L_1, L_2 - inductance of P/G pins

Figure 4. Model for ground bounce in internal circuits.

several inverters, large load capacitances, pin electronics, and power supply. As mentioned in [1], these models are not suitable for internal circuits. The model we will use to study ground bounce in internal logic is shown in Figure 4 and includes a large well/substrate capacitance C_s . This parasitic capacitance absorbs charge and hence reduces ground bounce. Designers often use de-coupling capacitors and/or filler cells to increase this capacitance. If this capacitance is neglected, the magnitude of ground bounce can not be correctly estimated.

3.2 Analysis of circuit model

In the following analysis, a falling output transition is assumed; the analysis for a rising output transition is similar.

Consider the circuit shown in Figure 4. It is reasonable to ignore the short-circuit current because in future technologies the supply voltage scales down faster than the transistor threshold voltages. By applying the Thevenin's and Norton's equivalent network theorems, an equivalent circuit can be obtained as shown in Figure 5. Assuming the waveform of current $I_n(t)$ through an N-type transistor is triangular with maximum value I_{nmax} [12], the current $I_n(t)$ is given by Equations (1)-(4).

Here t_r is the time required for the input signal to go from 0 to V_{dd} , t_0 is the time it takes $I_n(t)$ to go from I_{nmax} to 0, and $s=I_{nmax}/t_0$ is the slope of $I_n(t)$ in the range of I_{nmax} to 0. By applying Kirchoff's voltage and current laws to the circuit shown in Figure 5, the ground bounce $V_g(t)$ is derived as shown Equations (5) - (8), where

$$\begin{aligned} A &= \frac{C_p}{C_p + C_n} \\ s_r &= I_{nmax}/(t_r - t_n) \\ \omega &= 1/(\sqrt{2} \cdot L \cdot C) \\ b_1 &= L \cdot s_r \cdot (1 - \cos(\omega \cdot (t_r - t_n))) + L \cdot s \\ b_2 &= L \cdot s_r \cdot \sin(\omega \cdot (t_r - t_n)) \\ d_1 &= -(L \cdot s) + b_1 \cdot \cos(\omega \cdot t_0) + b_2 \cdot \sin(\omega \cdot t_0) \\ d_2 &= -b_1 \cdot \sin(\omega \cdot t_0) + b_2 \cdot \cos(\omega \cdot t_0) \end{aligned}$$

A plot of Equations (5) - (8) and SPICE level1 simulation with appropriate circuit parameters show that these two models lead to almost identical results.

Hence, the maximum magnitude of $V_g(t)$, V_{gmax} , is

$$V_{gmax} = A \cdot \left(-L \cdot s + \sqrt{(b_1^2 + b_2^2)} \right)$$

$$I_n(t) = \begin{cases} 0 & \text{if } 0 \leq t < (t_r \cdot V_{th}/V_{dd}) = t_n & (1) \\ I_{nmax} \cdot (t - t_n)/(t_r - t_n) & \text{if } t_r > t \geq t_n & (2) \\ I_{nmax} - s \cdot (t - t_r) & \text{if } (t_0 + t_r) > t \geq t_r & (3) \\ 0 & \text{if } t \geq (t_0 + t_r) & (4) \end{cases}$$

$$V_g(t) = \begin{cases} 0 & \text{if } t_n > t \geq 0 & (5) \\ A \cdot L \cdot s_r \cdot (1 - \cos(\omega \cdot (t - t_n))) & \text{if } t_r > t \geq t_n & (6) \\ A \cdot (-L \cdot s + b_1 \cdot \cos(\omega \cdot (t - t_r)) + b_2 \cdot \sin(\omega \cdot (t - t_r))) & \text{if } (t_0 + t_r) > t \geq t_r & (7) \\ A \cdot (d_1 \cdot \cos(\omega \cdot (t - (t_0 + t_r))) + d_2 \cdot \sin(\omega \cdot (t - (t_0 + t_r)))) & \text{if } t \geq (t_0 + t_r) & (8) \end{cases}$$

Often a designer attempts to have $t_r=t_0$, hence $s=s_r$, and by substitution, we get

$$V_{gmax} = L \cdot \frac{C_p}{C_p + C_n} \cdot \frac{I_{nmax}}{t_r - t_n} \cdot \left(-1 + \sqrt{5 - (4 \cdot \cos(\omega \cdot (t_r - t_n)))} \right)$$

Applying the Taylor series expansion to this form, we get

$$V_{gmax} = L \cdot \frac{C_p}{C_p + C_n} \cdot \frac{I_{nmax}}{t_r - t_n} \cdot \left((\omega \cdot (t_r - t_n))^2 + O(\omega \cdot (t_r - t_n)) \right) \quad (9)$$

where, $O(\omega \cdot (t_r - t_n))$ is the higher order term of Equation 9. Replacing ω with $1/\sqrt{2LC}$, and because $\omega \cdot t_r$ is much less than 1, the higher order term can be neglected, the following approximation can be obtained

$$V_{gmax} \cong \frac{C_p}{C_p + C_n} \cdot I_{nmax} \cdot \frac{1}{2 \cdot C} \cdot (t_r - t_n) \quad (10)$$

The form of Equation 10 gives us insight into the maximum magnitude of ground bounce as a function of circuit parameters. For example, the maximum magnitude of ground bounce is directly proportional to C_p , I_{nmax} , and $(t_r - t_n)$ and inversely proportional to C and $(C_p + C_n)$.

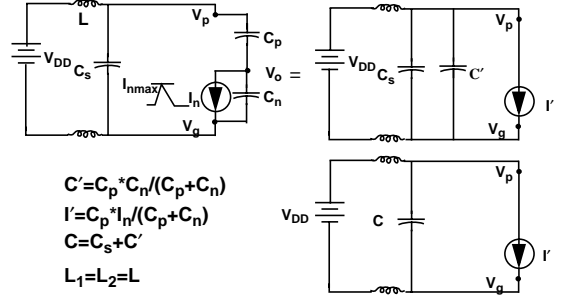


Figure 5. Equivalent circuits for circuit model.

3.3 Non-switching gate effect

If the output signal of an inverter is held at constant value "0", the equivalent circuit can be modeled as shown in Figure 6. From the equation for $V_g(t)$, the frequency of

ground bounce, $\omega = 1/\sqrt{2LC}$, is primarily determined by the pin inductance and the large substrate and on-chip decoupling capacitances. Because C is much greater than C_n and C_p , R_n is much less than $1/\omega C_n$ and $1/\omega C_p$, which are the equivalent impedances of C_n and C_p , respectively. The dominant effect in this case is that C_p behaves like a parallel connected capacitance to C , and by Equation 10 the reduced magnitude of ground bounce is approximately proportional to $(C^{-1} - (C + C_p)^{-1})$.

4. Cost function for ground bounce

4.1 Questions

The equations obtained above are based on some assumptions and simplified current equations. For developing a cost function to determining the real effect of circuit parameters on the magnitude of ground bounce, the following questions need to be answered: (1) what is the impact on ground bounce of falling vs. rising transitions; (2) what is the impact on ground bounce of gates where outputs have no transition; and (3) what is the impact on ground bounce of C_p and C_n ?

4.2 Experiments

To answer these questions, six series of experiments were performed. The first two were designed to identify the relationship between C_p , C_n and V_{gmax} (the maximum magnitude of ground bounce). The third and fourth series of experiments were used to determine the relationship between transistor width and V_{gmax} . The current is proportional to the gain factor of MOS transistor, which is usually proportional to transistor width. The last two series of experiments consider the effect of non-switching gates, which behave as decoupling capacitance, and hence reduce ground bounce.

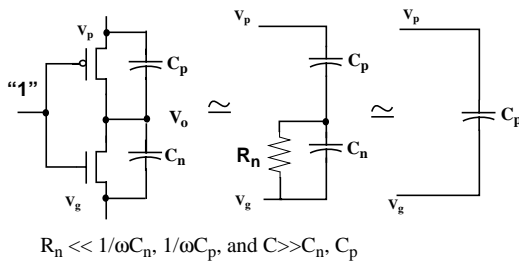


Figure 6. Equivalent circuits when gate output is held constant at logic 0.

A hypothetical chip with realistic assumptions was proposed in [1]. Based on the same assumption, we used 128

inverters connected in parallel in the experiments to determine the magnitude of ground bounce in internal logic. These inverters were connected to one power pin and one ground pin and switched simultaneously. In six series of experiments, MOSIS HP 0.8 μ m BSIM3v3 model parameters are used for transistors. The other parameters are listed next: the value of substrate capacitance, C_{sub} , is 20 pF; the rise/fall times (t_{0-vdd}/t_{vdd-0}) are 200 ps; W_p/W_n is assumed to be $16\lambda/8\lambda$ if not specified otherwise; and C_p and C_n are assumed to be 20 fF, respectively, if not specified otherwise. The pin electronics have a predominant influence on ground bounce. In our experiments, the pin electronics are based on the Pentium Pro chip [10]. Each pin is modeled using a four segment distributed RLC network, where the segments represent the bondwire, package trace, pin and socket. The detailed model and parameters are shown in Figure 7.

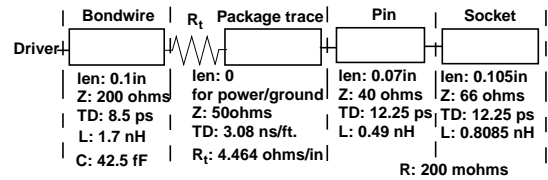


Figure 7. Pin electronics.

4.2.1 Experiments 1 and 2: C_p , C_n vs. V_{gmax} (output falling - F, output rising - R)

The first (second) series of experiments deal with the influence of C_p and C_n on V_{gmax} , when the gate output is falling (rising). The test circuit is shown in Figure 8. As

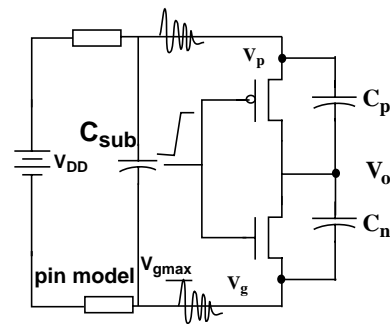


Figure 8. Test circuit for first four series of experiments.

the load capacitances C_p and C_n for each inverter vary, the maximum magnitude of ground bounce, V_{gmax} , is calculated and the results are summarized in Table 1.

TABLE 1. C_p , C_n vs. V_{gmax} (output falling - F, rising - R).

C_p (fF)	C_n (fF)	$V_{gmax}(F)$ (mV)	$V_{gmax}(R)$ (mV)
20	20	361.3	360.3
40	20	493.9	314.9
60	20	581.3	278.2
80	20	638.7	249.1
20	20	361.3	360.3
20	40	321.0	465.1
20	60	284.2	534.2
20	80	251.9	580.1

4.2.2 Experiment 3: $K_n(W_n)$ vs. V_{gmax}

This series of experiments was used to determine the impact of W_n on V_{gmax} . The load capacitances C_p and C_n are fixed as 20 fF. W_n is changed from 3.2 μ m to 12.8 μ m. The maximum magnitude of ground bounce when outputs are falling ($V_{gmax}(F)$) and rising ($V_{gmax}(R)$) are reported. The results are summarized in Table 2.

TABLE 2. W_n vs. $V_{gmax}(F)$ and $V_{gmax}(R)$.

W_n (μ m)	$V_{gmax}(F)$ (mV)	$V_{gmax}(R)$ (mV)
3.2	361.3	360.3
6.4	469.1	377.0
9.6	545.7	390.8
12.8	611.4	402.8

4.2.3 Experiment 4: $K_p(W_p)$ vs. V_{gmax}

These experiments are analogous to the previous ones, but now W_p varied from 6.4 μ m to 25.6 μ m. The results are shown in Table 3.

TABLE 3. W_p vs. $V_{gmax}(F)$ and $V_{gmax}(R)$.

W_p (μ m)	$V_{gmax}(R)$ (mV)	$V_{gmax}(F)$ (mV)
6.4	360.3	361.3
9.6	455.2	387.0
12.8	534.7	409.4
25.6	781.5	479.7

4.2.4 Experiments 5 and 6: effect of non-switching inverters

The purpose of the last two series of experiments were to determine how much the magnitude of ground bounce is reduced due to non-switching gates. The experiments are

setup as shown in Figure 9. Here two banks of inverters

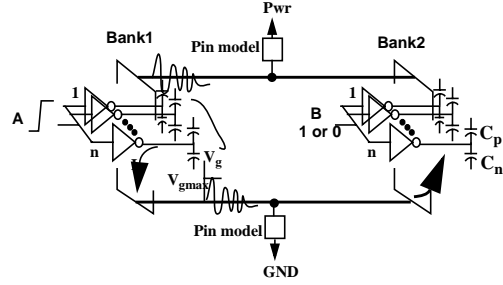


Figure 9. Test circuit for experiments 5 and 6 (n=128).

shared one power and one ground pin. Each bank has 128 inverters connected in parallel. The first bank of inverters have the same input, A, and each inverter has a load capacitance of $C_p=C_n=20$ fF. The second bank of inverters have the same input, B, and their load capacitances C_p and C_n can vary from 20 fF to 80 fF. The fifth series of experiments has A switching from 0 to 1 and the sixth series has A switching from 1 to 0. The maximum magnitude of ground bounce is measured first without the second bank of inverters, and then again while applying constant “0” or “1” to B. The results are summarized in Tables 4 and 5.

TABLE 4. C_p , C_n vs. $V_{gmax}(B=0)$, $V_{gmax}(B=1)$. For rising transition at A, no bank2 inverters, $V_{gmax}=361.3$ mV.

C_p (fF)	C_n (fF)	$V_{gmax}(B=0)$ (mV)	$V_{gmax}(B=1)$ (mV)
20	40	297.6	322.7
20	60	284.6	323.1
20	80	274.9	323.3
40	20	316.2	299.9
60	20	316.4	282.6
80	20	316.4	269.2

TABLE 5. C_p , C_n vs. $V_{gmax}(B=1)$, $V_{gmax}(B=0)$. For falling transition at A, and no bank2 inverters, $V_{gmax}=360.3$ mV.

C_p (fF)	C_n (fF)	$V_{gmax}(B=1)$ (mV)	$V_{gmax}(B=0)$ (mV)
20	40	324.0	298.7
20	60	324.4	285.1
20	80	324.7	274.9
40	20	301.6	317.6
60	20	284.0	318.0
80	20	269.9	318.2

4.2.5 Summary of experimental results

Based on equation 10, for an output falling transition, V_{gmax} is proportional to I_{nmax} and C_p and inversely proportional to (C_p+C_n) . The results of the first series of experiments shows that the maximum magnitude of ground bounce, V_{gmax} , increases when C_p increases, but decreases when C_n increases. The increasing rate of V_{gmax} when C_p increases is larger than its decreasing rate when C_n increases. This correlates well with equation 12. However, I_{nmax} also depends on the load capacitance (C_p+C_n) . By determining I_{nmax} via circuit simulations, it was observed that

$$I_{nmax} \propto \sqrt{(C_p + C_n)}$$

Hence,

$$V_{gmax} \propto \frac{C_p}{\sqrt{(C_p + C_n)}} \cdot \frac{1}{C}$$

From the results of experiments 3 and 4 when the output of the inverter is falling, V_{gmax} increases substantially when K_n increases, but increases a small amount when K_p increases. When the output is rising, K_n and K_p act in the opposite way. That is, $V_{gmax}(F)$ and $V_{gmax}(R)$ can be represented as

$$V_{gmax}(F) \propto \sqrt{K_n} + \varepsilon \cdot f(K_p)$$

$$V_{gmax}(R) \propto \sqrt{K_p} + \varepsilon \cdot f'(K_n)$$

From the results of experiments 5 and 6, the non-switching inverters (bank2) reduce the ground bounce generated by the switching inverters (bank1) and the observations are as follows: 1) when the outputs of the bank2 inverters are held at "0", the larger the value of C_p , the smaller is V_{gmax} , and C_n has little effect on V_{gmax} ; 2) when the outputs of the bank2 inverters are held at "1", the larger the value of C_n , the smaller is V_{gmax} , and C_p has little effect on V_{gmax} ; and 3) $V_{gmax}(B=1)$ and $V_{gmax}(B=0)$ have the following relationship

$$\frac{V_{gmax} - V_{gmax}(B=1)}{V_{gmax}} \leq \frac{C_p}{C \cdot (C + C_p)}$$

$$\frac{V_{gmax} - V_{gmax}(B=0)}{V_{gmax}} \leq \frac{C_n}{C \cdot (C + C_n)}$$

5. Algorithm to generate test patterns for maximum ground bounce in fan-out free circuits

5.1 Cost function

A signal line in a circuit can have a rising (R) transition, a falling (F) transition, be steady at 1 (P1), or steady at 0 (P0). Also switching lines contribute to ground bounce but non-switching lines dampen the ground bounce generated by switching lines. To generate test patterns for maximum ground bounce, these four phenomena must be considered and a cost function, which considers all the dominant parameters affecting the magnitude of ground bounce, must be determined to help direct the search process. Based on the previous analysis and experimental results, we can conclude that: 1) ground bounce is generated for both R and F output transitions; and 2) **the period of ground bounce, which is governed by pin electronics and the large de-coupling capacitance ($\approx 2.18ns$ in the experiments), is much greater than the gate delay ($\approx 200ps$)**. Hence, assuming shallow logic, ground bounce generated by gates in different levels between pipeline stages is additive. That is, the patterns generated for maximum ground bounce when ignoring the phase shift (delay) between the ground bounce generated by different levels of gates may be still a good approximation of the patterns that generate maximum ground bounce when considering all gate delays.

From our experimental results one cost function can be determined as follows:

Consider the following four local variables associated with a gate g.

I. Cost variables when output of gate g switches:

a) ΔR_g - contribution to ground bounce when output of g is rising:

$$\Delta R_g = a \cdot \frac{C_n}{\sqrt{(C_p + C_n)}} \cdot \sqrt{K_{peff}}$$

b) ΔF_g - contribution to ground bounce when output of g is falling:

$$\Delta F_g = b \cdot \frac{C_p}{\sqrt{(C_p + C_n)}} \cdot \sqrt{K_{neff}}$$

II. Fractional cost variables when output of g does not switch:

a) $\Delta P0_g$ - output of g is constant at 0:

$$\Delta P0_g = 1 - \frac{C_n}{C \cdot (C + C_n)}$$

b) $\Delta P1_g$ - output of g is constant at 1:

$$\Delta P1_g = 1 - \frac{C_p}{C \cdot (C + C_p)}$$

where a and b are constants and K_{peff} and K_{neff} are the effective gains of P-transistors and N-transistors, respectively, which depend on the input patterns, connections and transistor sizes.

5.2 Algorithm

Consider a fan-out free circuit and assume every gate is a CMOS gate implementing a unate function. Based on these assumptions, the following theorem can be proven.

Theorem 1 Given a transition at the output of an n input CMOS gate implementing a unate function, there exists an input vector pair (V_1, V_2) that implies the output transition and where each input line has a transition, i.e., $V = V_1 = \bar{V}_2$.

Proof: Assume the output transition is 0 to 1. One can always make a change of variables so that the unate function is positive in all variables. Then set $V_1 = (0, 0, \dots, 0)$.
Q.E.D.

Every signal line, λ , not only has four local variables as defined previously, but also has four global variables associated with it defined as follows: $R_\lambda(F_\lambda)$ - the maximum total contribution to ground bounce of the fan-in cone of line λ when λ is rising (falling); and $P0_\lambda(P1_\lambda)$ - the maximum total contribution to ground bounce of the fan-in cone of line λ when λ is held at 0(1). The basic strategy of the algorithm first requires a traversal of the circuit from inputs to outputs while accumulating the maximum contributions to ground bounce at each signal line based on the local cost of switching and fractional reduction due to non-switching. Figure 10 shows an AND gate and illustrates how the values of the four global variables associated with line c are computed. We will describe how R_c is computed; $P0_c$, $P1_c$, and F_c are computed in a similar way. There are three possible input patterns set c to R, namely $(a,b) = \{(R,R), (R,1), (1,R)\}$. R_c is the maximum of $\{(R_a + R_b + \Delta R_c), (R_a + P1_b + \Delta R_c'), (P1_a + R_b + \Delta R_c'')\}$, where, ΔR_c , $\Delta R_c'$, and $\Delta R_c''$ use the same generic formula for ΔR , but with different value of K_{peff} due to the different input patterns at a and b. Different kinds of gates will have their corresponding mapping functions. Once the four global parameters are known for the primary outputs, the maximum of the four values associated with each primary output is selected. By assigning these values to the outputs



$$P0_c = \max \{(P0_a + P0_b), (P0_a + P1_b), (P0_a + R_b), (P0_a + F_b), (P1_a + P0_b), (R_a + P0_b), (F_a + P0_b), (R_a + F_b), (F_a + R_b)\} * \Delta P0_c$$

$$P1_c = (P1_a + P1_b) * \Delta P1_c$$

$$R_c = \max \{(R_a + R_b + \Delta R_c), (R_a + P1_b + \Delta R_c'), (P1_a + R_b + \Delta R_c'')\}$$

$$F_c = \max \{(F_a + F_b + \Delta F_c), (F_a + P1_b + \Delta F_c'), (P1_a + F_b + \Delta F_c'')\}$$

where,

$\Delta R_c, \Delta R_c',$ and $\Delta R_c''$ use the same formula as ΔR , but with different K_{peff} due to different input patterns at a and b

Figure 10. A demonstration of how to compute variables of an AND gate.

and by Theorem 1, the input values of the gates driving the primary outputs can be determined. In the same fashion we continue this back-trace process until the primary inputs are reached. The detailed algorithm is described as follows.

1) Compute C_p and C_n for each gate based on physical information and circuit netlist.

2) Apply initial condition for primary inputs: $P0=P1=0$, $R=\Delta R$ and $F=\Delta F$ whose values are determined by their input drivers.

3) Compute the values of $P0$, $P1$, R , and F by the method shown in Figure 11 for the output of each gate starting from the first level of gates until reaching the primary outputs.

4) Choose $\max(P0, P1, R, F)$ for each primary output.

5) Back-trace to obtain the test patterns.

5.1) Assigning primary output value as $\max(P0, P1, R, F)$ for each primary output.

5.2) Determine the value of each line going from outputs to inputs until the primary inputs are reached.

The details regarding how the input values are determined are shown in Figure 11. In this example, from the computed values, assume R_c is the maximum of $(P0_c, P1_c, R_c, F_c)$. Therefore R is assigned to c. In step 3 of the algorithm, we know R_c is the value corresponding to $a=R$ and $b=R$, so R is assigned to a and b.

5.3) The obtained patterns at the primary inputs represent the test for maximum ground bounce.

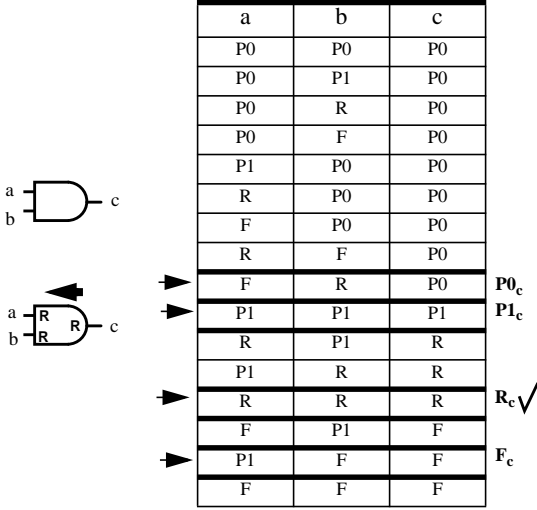


Figure 11. An example demonstrates how back-trace is performed to obtain input patterns.

5.3 Experimental results

Next we apply the above algorithm to the simple circuit shown in Figure 12. The obtained input pattern is (F, F, R, R). Several SPICE simulations were performed to verify the results.

TABLE 6. Experimental results of circuit shown in Figure 12.

1	2	3	4	# of trans. in circuits	V_{gmax} (mV)
F	F	R	R	8	5.458
R	R	F	F	8	5.086
F	F	F	F	7	5.331
F	F	F	R	7	4.522
R	R	R	F	7	3.307
R	F	F	F	6	3.786
F	R	R	F	4	2.105

From the simulation results shown in Table 6, the test (F, F, R, R) did generate the largest ground bounce of all the patterns considered. Note that the maximum value of ground bounce does not necessarily increase monotonically with the number of transitions in the circuits (shown in column 5 of the table). For example, the input pattern shown in the third row of Table 6 generated a larger ground bounce than the one in the second row. Based on the physical information and circuit netlist, C_p of line 6 and 7 are much greater than the corresponding values of C_n . From our cost function, we know that ΔF_6 and ΔF_7 are much greater than ΔR_6 and ΔR_7 . That is, to generate a large ground bounce, a falling transition at lines 6 and 7 is

more desirable than a rising transition. Hence, even though the pattern in the third row has less transitions than that in the second row, it generates a larger ground bounce.

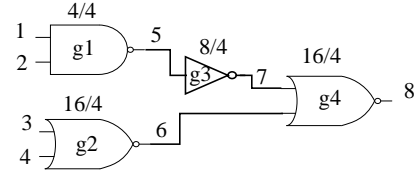


Figure 12. A simple fan-out free circuits for generating tests and simulation.

To evaluate our algorithm on large combinational circuits, some ISCAS-85 and MCNC benchmark circuits were modified to become fan-out free circuits. Every node with more than one fan-out in a circuit was cut and connected to its first fan-out node. Its other fan-out nodes were changed to become primary inputs. The above algorithm was implemented and applied to these test cases. For purposes of comparison, two other types of test patterns were generated. One (tests A) was generated by randomly assigning either R or F to the primary outputs and performing a back-trace to obtain input patterns. From Theorem 1, such patterns can cause transitions at all circuit lines. The other (tests B) was generated using a random test pattern generator which randomly assigned primary inputs with R or F. These three types of patterns are applied to all example circuits, and the SPICE simulation results are shown in Tables 7 and 8.

TABLE 7. Experimental results for ISCAS-85 circuits. (voltage unit: mV).

ckts(lines)	our tests	no. of trans.	Avg. of Tests A	Avg. of Tests B
c17(14)	12.61	14	12.50	9.185
c432(343)	389.2	343	376.88	335.98
c880(755)	432.7	750	428.80	320.3
c1355(1096)	558.1	1096	589.15	490.20
c1908(1523)	742.0	1523	770.20	671.83
c3540(2961)	1045	2945	994.66	734.40

TABLE 8. Experimental results for MCNC benchmark circuits. (voltage unit: mV).

ckts(lines)	our tests	no. of trans.	Avg. of Tests A	Avg. of Tests B
bw(196)	229.8	196	228.3	147.6
f2(24)	29.45	24	29.17	20.07
alupla(184)	207.7	183	225.02	198.52

5.4 Discussions

From the simulation results, the test patterns generated by our algorithm produce either maximum ground bounce or very close to the ground bounce produced by maximum switching activity. We believe we do not always generate the worst case test pattern because (1) we assumed a zero-delay model and (2) some gates have large (>5) fan-ins. The assumption of zero-delay model will lead to an accurate analysis only if the designs are shallow logics. Some of test cases have more than 50 level of logics. Also, internal node capacitances are neglected in our algorithm. For large fan-in gates, the charge stored in these capacitances may have large contributions to ground bounce. These effects can be included in our model.

6. Circuits without re-convergent fan-out

6.1 Rationale

When a circuit has fan-out, the algorithm given previously cannot be directly applied. The reason is that because of the inversion polarity of different branches, assigning values to the outputs coming from the same fan-out node may lead to conflicts in the back-trace process. For example, as shown in Figure 13, assigning R to both node 30 and 32 causes a conflict in the fan-out node 25. The previous algorithm can be modified to account for this situation.

6.2 Algorithm

To resolve conflicts at fan-out nodes, only one variable at a time is considered when the traversal from inputs to outputs reaches a fan-out node. For the circuit shown in Figure 13, line 25 has fan-out. Considering gate 10, the four variables associated with line 31 are computed by setting line 25 to a fixed value, (P0, P1, R, or F) - chosen one at a time. For example, when setting line 25 to R and the other three variables associated with line 25, namely, P0₂₅, P1₂₅, and F₂₅, are set to be invalid. Performing an operation of + or * in an invalid variable produces an invalid result. The max operator will select the maximum of valid variables. In this case, only F₃₁ and P1₃₁ are valid for line 31 and F₃₁ is the maximum of $\{R_{28}+P1_{26}+\Delta F_{31}', R_{28}+R_{26}+\Delta F_{31}\}$. Here, the value of R₂₈ is set to 0 and it will be added later to the total cost. The reason that the value of R₂₈=R₂₅ is added in the final stage is that otherwise, the value of R₂₅ will be added twice because gate 5 and 10 both depend on line 25. In this fashion, the variables associated with line 30 and line 32 are computed. We select the maximum global variable for each output line

from the valid ones. Then we take the sum of the values of the selected variables and R₂₅. This summation is called the total contributions to ground bounce when line 25 is R, namely, Cost(R₂₅). In a similar fashion, the other three total contributions, Cost(P0₂₅), Cost(P1₂₅), and Cost(F₂₅), can be obtained. The maximum of Cost(P0₂₅), Cost(P1₂₅), Cost(R₂₅), and Cost(F₂₅) is selected and the value for each primary output is determined. The same back-trace method as in Section 5 is performed to obtain input patterns.

7. Circuits with re-convergent fan-out

For circuits with re-convergent fan-out, the same algorithm proposed in Section 6 can be applied to obtain test patterns. To reduce the computational complexity, the concept of supergate can be used. In [11], a supergate of a node X, denoted as SG(X), is defined to be the minimal circuit substructure necessary to compute the controllability value at node X. Such circuits can be used to hide the effects of re-convergence. In our case, SG(X) with its associated four variables can be used to compute the cost of its succeeding gates. The supergate of a re-convergent node can be treated as a large gate implementing a complex function. For example, an XOR function can be implemented with inverter, AND, and OR gates as shown in Figure 14, which is a circuit with re-convergent fan-out. By the definition of supergate, SG(X) can be treated as a large gate implementing an XOR function which has inputs a and b. The local cost of such a supergate, $\Delta P0$, $\Delta P1$, ΔR , and ΔF , can be computed with the methods proposed in Section 6. Then, these supergates are treated the same as other primitive gates and our algorithm can be applied as well. However, if the supergates are too large, such as greater than four levels of primitive gates, this method may not be that useful, because the complexity will be close to the one in Section 6.

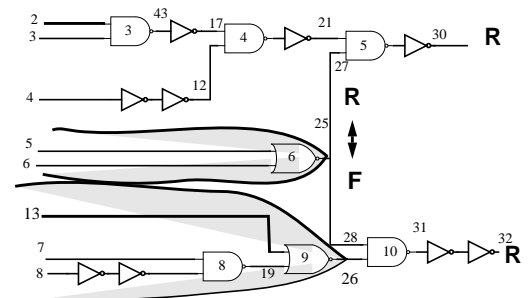


Figure 13. A circuit without re-convergent fan-outs may have conflict in node 25 in back-trace stage.

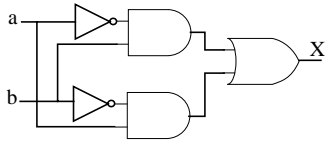


Figure 14. An XOR implemented with inverters, AND and OR gates.

8. Conclusions

A new circuit model for ground bounce in internal logic is proposed. From this model, its associated analytic equation and circuit simulations, a cost function that considers the dominant circuit parameters that affect ground bounce is derived. Based on this cost function, an algorithm is presented for generating test patterns that maximizes ground bounce due to switching in combinational logic. For fan-out free circuits, we verified our results using SPICE simulation. The algorithm has been modified to consider circuits with and without re-convergent fan-out. Though the results matched our predicted results, more analysis is needed to determine the quality of the result.

The test generated by our algorithms consists of a pair of input patterns that do indeed produce the maximum ground bounce in a circuit having shallow logic. This test can help designers validate their designs in the presence of ground bounce. Our cost function can be used to identify sites in a circuit at which ground bounce may cause logic errors. The test also provides a good estimation of the magnitude of ground bounce that can be used to help determine a maximum value of circuit delay. Our test generation algorithm can be combined with more classical algorithms as described in Section 2 to produce tests for both validation and post manufacture testing.

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